INSTRUCTION MANUAL

MODEL 755-S-271 PROGRAMMABLE PHASE METER

WAVETEK

9045 BALBOA AVENUE, SAN DIEGO, CALIFORNIA

Serial No. _____

INSTRUCTION MANUAL

MODEL 755-S-271
PROGRAMMABLE
PHASE METER

Any reference in this manual to Model 755-S-206 or Model 755-S-206A should be read as Model 755-S-271. Any reference to Model 157-S-140 should be read as Model 157-S-272.

See the Model 755-S-271 Addendum.

WAVETEK
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2/73

- Zero Crossing Board Assembly 352-011 and Schematic 352-211 drawings. Change the Parts List and schematic values as follows:

Item	Ref Des	Description	Mfgr	Mfgr No.	Qty
10	C136 – C139	Silver Mica, 500 V, 5%, 1500 pF	ARCO	CM06FD152J03	4
20	C1, 5, 64, 68	Variable Capacitor, 3 pF - 12 pF	ERIE	503-001-17A	4

Product Improvement Notice

Wavetek maintains a continuing program to make improvements to their instruments that will take advantage of the latest electronic developments in circuitry and components.

Due to the time required to document and print instruction manuals, it is not always possible to incorporate these changes in the manual.

Wavetek has manufactured your instrument, using metal film 1% tolerance resistors in place of 5% carbon resistors, wherever practical. This results in a substantial improvement in the overall performance of your instrument. Therefore, there may exist a discrepancy between the resistor used to manufacture your instrument and the resistor called out in the Parts List and Schematic Diagrams in this manual.

If field replacement of an affected resistor does become necessary, replacement may be made in accordance with the manual call outs. Wavetek, however, recommends replacement with the same type of resistor used in the manufacture of your instrument, whenever possible.

CONTENTS

SECTION 1 – INTRODUCTION

1.1 PURPOSE OF THE EQUIPMENT 1-1
1.2 SPECIFICATIONS PHASE MEASUREMENT 1-2
1.3 SPECIFICATIONS OF PHASE LOCK 1-3
1.4 SPECIFICATIONS GENERAL 1-4

SECTION 2 – INSTALLATION AND OPERATION

2.1 MECHANICAL INSTALLATION 2-1
2.2 ELECTRICAL INSTALLATION 2-1
2.3 OPERATING CONTROLS 2-5
2.4 PRELIMINARY CHECKS 2-6
2.5 OPERATION PROCEDURE 2-7

SECTION 3 – CIRCUIT DESCRIPTION

3.1 SIMPLIFIED BLOCK DIAGRAM 3-1
3.2 FUNCTIONAL BLOCK DIAGRAM ANALYSIS 3-2
3.3 SUPPLEMENTAL CIRCUITS 3-11

SECTION 4 – MAINTENANCE

4.1 ACCESS INSTRUCTIONS 4-1
4.2 CALIBRATION INSTRUCTIONS 4-1
4.3 CORRECTIVE MAINTENANCE 4-9

SECTION 5 – DIAGRAMS, ADDENDUMS AND PARTS LIST

5.1 DIAGRAMS 5-1
5.2 ADDENDUMS 5-1
5.3 PARTS LIST 5-1

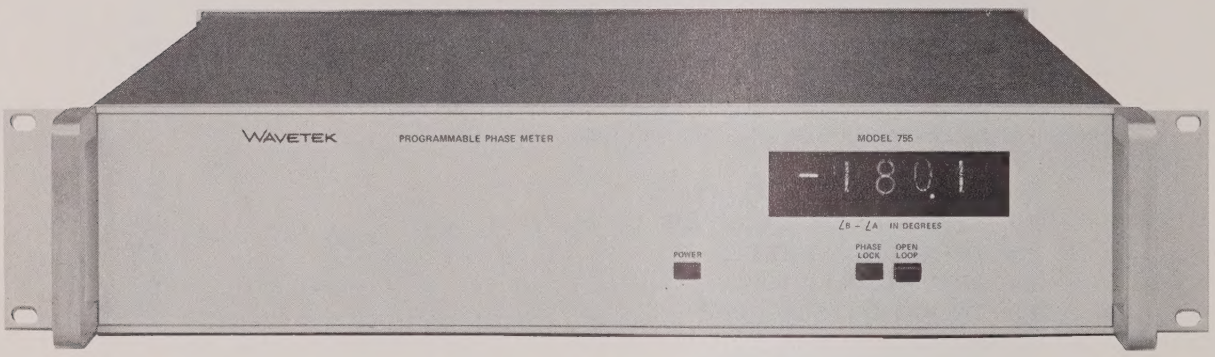

Figure i Model 755-S-206 Programmable Phase Meter

SCOPE OF THIS MANUAL

This manual provides descriptive material and instructions for the installation, operation, maintenance, and repair of this instrument. Wavetek's product improvement program ensures that the latest electronic developments are incorporated in all Wavetek instruments by the addition of circuit and component changes as rapidly as development and testing permit. Due to the time required to document and print instruction manuals, it is not always possible to incorporate the more recent changes in the released manual. In this case, data will be found on engineering change sheets at the rear of the manual. If no change sheets are included, the manual is correct as printed.

INSTRUCTION MANUAL ADDENDUM
FOR
Model 755-S-206A
1/75

The following changes are to be incorporated into the 755-S-206A Programmable Phase Meter to increase the stability and accuracy of the phase lock loop. The Instruction Manual should be Red Lined to show the following changes:

Page 4-4
4.2.5 Zero-Crossing Mid-Frequency Procedure
Insert after number 27

27a. Center R82 on channel "A" and center R173 on channel "B".

CAUTION

DO NOT ADJUST THESE POTS DURING CALIBRATION AFTER CENTERING THEM.

Page 4-7
4.2.7 Phase Lock Calibration Procedure
Replace 80 and 81 with the following. Delete 82 through 87.

80. Place the(+)probe of a dc voltmeter on the wiper of R54 and the(–)probe on circuit ground. Adjust R54 for +0.7 V ±0.1 Vdc.

81. Place the(–)probe of the dc voltmeter on the wiper of R21 and the(+)probe on circuit ground. Adjust R21 for –0.7 V ±0.1 Vdc.

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SECTION 1
INTRODUCTION

1.1 PURPOSE OF THE EQUIPMENT

The WAVETEK Model 755-S-206 PROGRAMMABLE PHASE METER is an automatic programmable phase meter especially designed for use in systems applications. The features of the Model 755-S-206 include the following:

- Automatic Ranging (measurement)/Programmable Range BCD Output(s)
- External Read Command — which allows the system to update its digital readout only on command from an external source.
- Programmable Calibrate Command
- Program Isolation
- Programmable Amplitude Range
- Phase Lock Operation
- Phase Shift Programming

1.1.1 Measurement Mode

The Model 755-S-206 Programmable Phase Meter has been designed to accurately measure the phase angle between any two ac signals (with an amplitude dynamic range up to 1000 to 1) within the 40 Hz to 2 MHz range. A precision wideband instrument, the Model 755-S-206 uses a unique circuit design which permits accurate phase angle measurement with input signals having high even harmonic distortion. A four-digit readout is used to display, in degrees and tenths of degrees, the angle being measured.

Two ranges, 0°/360° and −180°/+180°, assure continuous phase data without discontinuity at 0 and 180 degrees. The auto ranging circuit incorporated in the Model 755-S-206, automatically changes the range to permit the best possible operation to alleviate the phase discontinuity problem. High impedance differential inputs are used; and a dc OUTPUT −10mV/DEG is provided for use in recording phase angle measurements, or as a control signal for phase lock loops or servo systems. The BCD output is available on the rear of the instrument. Also the phase max-min calibrate programming is available which allows the user to program the maximum and minimum of the range selected to be read out on the digital display.

The automatic operation of this instrument eliminates the need for amplitude matching, frequency tuning, and output filtering, resulting in true hand-off phase measurements.

1.1.2 Phase Lock Mode

The Model 755-S-206 includes a phase lock feature which allows the instrument to be used as the phase detection and control portion of a phase-lock loop. When used in conjunction with a voltage-controlled oscillator, the Model 755-S-206 can be used to phase-lock and phase shift an external frequency to the VCO. Phase modulation and frequency modulation can be accomplished by voltage-controlled programming. For precise phase-locking and phase-shift programming, the Model 755-S-206 Phase Meter may be used with the Wavetek Model 157-S-140 Waveform Synthesizer.

When used with the Model 157-S-140, the Model 755 can phase-lock the Model 157-S-140 to an external frequency. Discrete phase shifts may then be programmed, providing truly precise phase shifts between the Model 157-S-140 output and the external frequency selected.

The standard discrete phase shift program points are zero degrees, +30 degrees, −30 degrees, +90 degrees, −90 degrees, and 180 degrees. Beside the discrete phase-shift program points, a continuous dc voltage may be used to continuously control the phase shift from zero to 360 degrees.

When used in a phase-lock configuration with the Model 157-S-140, two pushbuttons on the front panel of the Model 755-S-206 (labeled "PHASE LOCK" and "OPEN LOOP") are used to phase-lock the Model 157-S-140 via the Model 755-S-206 or allow both the Model 157-S-140 and the Model 755-S-206 to be used separately.

Another programming feature in the phase-lock mode is the time constant programming—which allows the loop filter of the phase-lock loop to be programmed for different frequency ranges.

1.2 SPECIFICATIONS PHASE MEASUREMENT

1.2.1 Input Signals

Frequency Range . . . . . 40 Hz to 2 MHz

Absolute Calibration Accuracy
200 Hz to 20 kHz square wave, 100 mV to 5 V p-p . ±0.1°

Frequency Effect on Accuracy (100% of Range Sine Wave Inputs)
200 Hz to 20 kHz . . . . Calibration Accuracy ±0.2°
Zero Offset, 40 Hz to 10 kHz . . . . .Less than 0.1°
Zero Offset, 10 kHz to 100 kHz . Less than 0.1°/10 kHz
Relative Accuracy, 100 kHz to 2 MHz . Better than 2°
Ripple due to decreased time constant is approximately 0.4° at 100 Hz, 0.6° at 50 Hz and 2° at 40 Hz.

NOTE

Program time constant **IN** *for phase measurements by connecting loop time constant BCD connector (J2) pin (32) to program ground pin (25).*

OVERVOLTAGE LIMITS

Amplitude Ranges	AC Limit	Maximum Peak (AC + DC Limit)
.001-2 VOLTS RMS . . .	300 V RMS . .	300 VOLTS
.300-300 VOLTS RMS . .	330 V RMS . .	500 VOLTS

Amplitude Effect on Accuracy (Equal Level Inputs)
Less than 1.5° for 60 dB change on both (A and B) inputs.

NOTE

1. *Minimum sensitivity above 50 kHz is 1% of full scale selected.*
2. *For frequencies above 20 kHz, both channel A and channel B should be programmed to the same range to eliminate attenuator phase delay.*

Phase Angle Resolution . . . . . 0.1°
Phase Angle Drift . . . . . Less than 0.3°/100 hours

Input Impedance
Single-Ended Inputs . . . . .1 MΩ, shunted by 30 pF
Differential Inputs . . . . .2 MΩ, shunted by 20 pF

Common Mode Rejection
40 Hz to 100 kHz . . . . . .Greater than 50 dB
100 kHz to 2 MHz . . . . . Greater than 40 dB

1.2.2 Readout/Controls

Display
Four digit Nixie readout −180.0° to +360.0° with automatic lead-lag (+ and −) indication.

All phase angle measurements are dependent on type of waveform, amplitude, and frequency. The diagrams below show the absolute accuracy, taking into account all sources of error.

ABSOLUTE ACCURACY
40 Hz-100 kHz

ALL ACCURACIES STATED ARE ± DEGREES

CHANNEL A AMPLITUDE PERCENT OF FULL SCALE	.1%	1%	10%	100%
100%	2.4	1.5	0.7	0.4
10%	1.5	0.7	0.6	0.7
1%	0.7	1.0	0.7	1.5
.1%	1.5	0.7	1.5	2.4

CHANNEL B AMPLITUDE PERCENT OF FULL SCALE

The term relative accuracy means the accuracy of difference in phase reading from one condition to another. For example, it is the accuracy of 1) repeatability, 2) comparison of readings among unknown signals with respect to a given signal, 3) phase deviation of input without regard to zero offset.

MULTIPLICATION FACTOR
AS A FUNCTION OF FREQUENCY

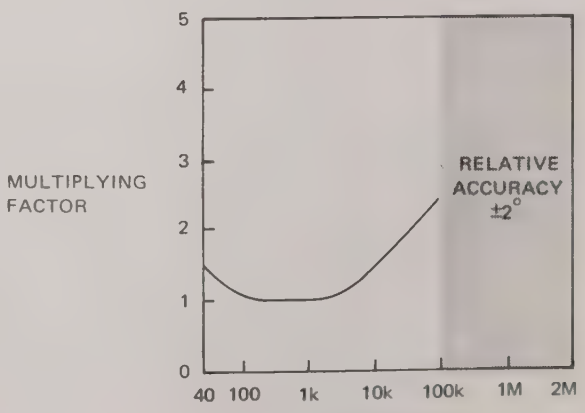


Figure 1-1. Instrument Accuracy Diagrams

Phase Ranges

Selected . . . . . 0/360°
Selected . . . . . −180°/+180°

NOTE

Phase measurements within 5° of Range Limit —Not specified.

Auto Range . . . . . 0°/360 or −180°/+180°

NOTE

Unit will auto range within approximately 10 to 20 degrees of range limit.

1.2.3 Analog (Recorder Output)

OUTPUT −10 mV/DEG

Amplitude, 0°/360° Range . . 0 Vdc to −3.600 Vdc
Amplitude, −180°/+180° Range .+1.8 Vdc to −1.8 Vdc
Output Impedance . . . . . 1 kΩ

BCD OUTPUT

Logic 1 . . . . . Contact closure to Program Ground
Logic 0 . . . . . Open
Output Coding. 8-4-2-1

1.2.4 Response Time (Full Scale Change)

Analog

Less than 4 seconds

Digitizing Time

1 second maximum.

Auto-Ranging

2 seconds.

1.2.5 Programming Controls

Read Command Input

Accepts negative going pulse 2-10 V, 100 nanoseconds minimum width. Continuous read command available with rear panel switch.

Print Command Output

Pulse 0(±.4 V) to 2.4 V nominal when reading is available. Minimum width 50 microseconds.

1.3 SPECIFICATIONS PHASE LOCK

1.3.1 Input Signals

Frequency . . . . . 200 Hz to 10 kHz

Discrete Capture Frequencies . . . . . 400 Hz ±10%
800 Hz ±10%
1.6 kHz ±10%
6.3 kHz ±10%

NOTE

Even though discrete frequencies are specified, the phase lock loop will operate over a wider continuous frequency range. However, the operator should note distortion introduced at extreme lower limits and capture frequency limitations at higher limits.

Capture Range (Frequency)

Frequency difference of reference, and controlled frequencies . . . . . ±2% max.

CAPTURE RANGE is defined for zero degrees phase shift on the ±180 degree range and for 180 degrees phase shift on the 0/360 degree range.

Phase Lock Range (Frequency)

After the phase lock loop has captured the controlled frequency, it will hold the lock for a frequency difference of ±10% or less for any single, discrete, programmed phase shift.

NOTE

Program low time constant for frequency 600 Hz and below.

Capture Range Amplitude

Slave Amplitude . . . 10% — 100% of Amplitude Range
Reference Amplitude . 1% — 100% of Amplitude Range

Phase Lock Hold Amplitude

After the phase lock loop has captured the controlled frequency, it will hold the lock with an amplitude input, (on both Channel A and Channel B) within normal range limits .001 — 2 V RMS; .300 — 300 V RMS.

1.3.2 Accuracy

Phase Lock Accuracy

Phase measurement accuracy at specified frequency plus an additional factor of ±0.5° for each 1% frequency difference between the reference frequency and the programmed frequency of the controlled 157.

1.3.3 Controls

Programmable Discrete Phase Shifts

±30°, ±90°, and 180°.

Continuous Phase Shift Control
±100 mV per degree.
100 k ohm impedance.

1.3.4 Phase Shift Programming

±180° Range . . . . . Frequency capture at zero degrees then phase shift discrete ±30°, ±90° or analog ±12 V max. (±120° relative to zero degrees max.)

0/360° Range . . Frequency capture at 180 degrees then phase shift discrete ±30°, ±90° or analog ±12 V max. (±120° relative to 180 degrees max.)

1.4 SPECIFICATIONS GENERAL

1.4.1 Input Isolation

All input and output signals, except recorder output and continuous phase shift control are isolated from circuit ground by 50 MΩ measured with a maximum of 100 Vdc.

NOTE

For true input isolation, the differential inputs should be utilized with the shield tied to the BNC common at the 755 end only. This is connected to the 755-S-206 circuit ground.

1.4.2 Environmental Characteristics (Specifications Apply)

Recommended Warmup . . . . . 30 minutes
Temperature . . . . . 20°C to 30°C
Relative Humidity . . . . . 30% to 75%

1.4.3 Mechanical

Dimensions
19 inches wide, 3-½ inches high, 16-½ inches deep.

Weight
14 lb. net, 24 lb. shipping.

Power Requirements
105 – 125 Vac or 200 – 250 Vac, 50 Hz to 400 Hz less than 35 watts.

Connector:
- BCD Output – Amphenol 57-40360
- Phase Program – Amphenol 57-40360
- Phase Lock – Amphenol 126-215-1000 or Winchester M4P-LSH10
- Input – BNC (female)

Mating Connectors:
- BCD Output – Amphenol 57-30360
- Phase Program – Amphenol 57-30360
- Phase Lock – Amphenol 126-214-1002 or Winchester M4S-LRN
- Input – BNC (male)

SECTION 2
INSTALLATION AND OPERATION

2.1 MECHANICAL INSTALLATION

After unpacking the instrument, visually inspect the external parts for damage to switches, indicators, connectors, surface areas, etc. If damage is discovered, file a claim with the carrier who transported the unit. The shipping container and packing material should be saved in case reshipment is required.

The front panel has been designed to allow this unit to be mounted in a standard 19-inch equipment rack. No mechanical installation is required when the instrument is to be used as a portable bench unit.

2.2 ELECTRICAL INSTALLATION

2.2.1 Power Connection

Connect the ac line cord to the mating connector at the rear of the unit and to the ac line supply. Check that the proper type of fuse is installed for the line supply being used.

NOTICE

Unless otherwise specified at the time of purchase, all Wavetek instruments are shipped from the factory with the power transformer connected for operation on a nominal 115-volt ac line supply, and a ½ amp 115 V line fuse.

NOTICE

Conversion for 230-volt operation requires resetting the 115/230 conversion switch at the rear of the instrument. Set the slide switch to 230, and install a fuse with a rating of ¼ amp at 230 volts.

2.2.2 Input Connections

Connect the desired input signals to their respective connectors using shielded cable equipped with female BNC connectors. Connect single-ended inputs to the appropriate polarity BNC, with the grounding cap on the opposite polarity BNC. Connect differential inputs between the "+" and "–" BNC, and disconnect the grounding cap. See Table 2-1 for input connections and there requirements.

Table 2-1. ELECTRICAL INSTALLATION GUIDE

Symbol	Name	Function	
J1	(Line Cord)	Connector for 3-wire line cord.	
J2	BCD Output	BCD Output Connector (See Table 2-2).	
J3	Input A "+"	Connectors for single-ended or differential input signal. The grounding cap is used only with single-ended input.	Observe amplitude specifications and limits of paragraph 1.2.
J4	Input A "–"		
J5	Input B "+"	Connectors for single-ended or differential input signal. The grounding cap is used only with single-ended input.	Use shielded cables with BNC connectors for these connections.
J6	Input B "–"		
J7	Phase Lock	Interconnection to slave 157 for phase lock operation.	
J8	Phase Program	Phase Program Connector (See Table 2-3).	

TABLE 2-2 MODEL 755-S-206 BCD OUTPUT CONNECTOR PIN LOCATION

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36
1 2 4 8 TENTHS				1 2 4 8 UNITS				1 2 4 8 TENS				1 2 HUNDREDS		±	READ COMMAND IN	RECORDER OUTPUT	CIRCUIT GROUND	PRINT COMMAND OUT	RANGE PROGRAM	RANGE MINIMUM CALIBRATE	RANGE MAXIMUM CALIBRATE	CHANNEL 'A' AMPLITUDE PROGRAM	CHANNEL 'B' AMPLITUDE PROGRAM	PROGRAM GROUND	-30° PROGRAM	-90° PROGRAM	+30° PROGRAM	+90° PROGRAM	AUTO RANGE/RANGE SELECT PROGRAM	+180° PROGRAM	LOOP TIME CONSTANT	CONTINUOUS PHASE SHIFT CONTROL	PHASE LOCK PROGRAM		

Pin No. Description

1-14 BCD OUTPUT — Logic 1 = Contact closure to program ground.
Logic 0 = Open
8421 output code.

15 ± Indicating the signal on Channel B is leading the signal on Channel A for (+) and lagging the signal on Channel A for (—).
+ = Contact closure to program ground
— = Open

16 READ COMMAND IN — When a negative going pulse of 2 to 10 volts and a minimum width of 100 nanoseconds is applied to this pin; the system will update its reading if in the external read command mode.

17 RECORDER OUTPUT — A dc voltage proportional to the phase reading is available between this pin and CIRCUIT GROUND pin (18). —10 mV/degree from 1 kΩ impedance.

Pin No. Description

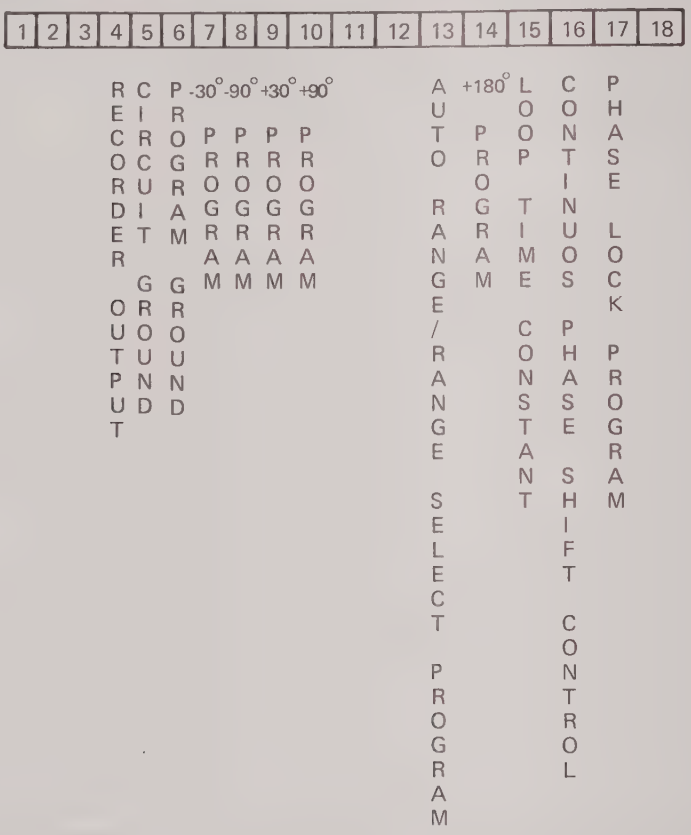
18 CIRCUIT GROUND — Reference for RECORDER OUTPUT pin (17) and CONTINUOUS PHASE SHIFT CONTROL pin (33). The CIRCUIT GROUND is isolated from PROGRAM GROUND.

19 PRINT COMMAND OUT — A pulse of 2.4 volts nominal with a minimum width of 50 microseconds will be applied to this pin when the BCD data is available.

20 RANGE PROGRAM — This function allows the programming of the phase range, either 0/360° or —180°/+180° range, IF the AUTO RANGE/RANGE SELECT is in the RANGE SELECT position and the 0/360° —180°/+180° or EXT PROGRAM is in the —180°/+180° or EXT PROGRAM position. An open or 0 volt ±0.4 volt will place the instrument in the —180°/+180° range. A +2.4 volts will place the instrument in the 0/360° range. Voltages are referenced to PROGRAM GROUND pin (25).

Pin No.	Description
21	RANGE MINIMUM CALIBRATE – This selects the minimum phase detector range extreme, either –180° or 0°, to appear on the display and BCD OUTPUT so the phase detector and digital readout calibration can be checked. An open or +2.4 volts will inhibit this mode. A PROGRAM GROUND pin (25) ±0.4 volts will select this calibrate mode. The voltages are referenced to the PROGRAM GROUND pin (25).
22	RANGE MAXIMUM CALIBRATE – This selects the maximum phase detector range extreme, either +180° or 360°, to appear on the display and BCD OUTPUT so the phase detector and digital readout calibration can be checked. An open or +2.4 volts will inhibit this mode. A PROGRAM GROUND pin (25) ±0.4 volts will select this calibrate mode. The voltages are referenced to the PROGRAM GROUND pin (25).
23	CHANNEL A AMPLITUDE PROGRAM – Allows the selection of one of two ranges. An open or +.24 volts allows .300 - 300 volts rms input sensitivity. A PROGRAM GROUND pin (25) ±0.4 volts allows .001 - 2 volts rms input sensitivity. The voltages are referenced to the PROGRAM GROUND pin (25).
24	CHANNEL B AMPLITUDE PROGRAM – Allows the selection of one or two ranges. An open or +2.4 volts allows .300 - 300 volts rms input sensitivity. A PROGRAM GROUND pin (25) ±0.4 volts allows .001 - 2 volts rms input sensitivity. The voltages are referenced to the PROGRAM GROUND pin (25).
25	PROGRAM GROUND – Is isolated from CIRCUIT GROUND pin (18) circuit common and is tied to power ground. All program voltages are referenced to PROGRAM GROUND.
26	–30° PROGRAM – Discrete phase shift program. If this pin is grounded to PROGRAM GROUND pin (25) ±0.4 volts, the output waveform will lag the reference by 30°. A +2.4 volts or open will inhibit this phase shift. All program voltages are referenced to PROGRAM GROUND.
27	–90° PROGRAM – Discrete phase shift program. If this pin is grounded to PROGRAM GROUND pin (25) ±0.4 volts, the output waveform will lag the reference by 90°. A +2.4 volts or open will inhibit this phase shift. All program voltages are referenced to PROGRAM GROUND.
28	+30° PROGRAM – Discrete phase shift program. If this pin is grounded to PROGRAM GROUND pin (25) ±0.4 volts, the output waveform will lead the reference by 30°. A +2.4 volts or open will inhibit this phase shift. All program voltages are referenced to PROGRAM GROUND.
29	+90° PROGRAM – Discrete phase shift program. If this pin is grounded to PROGRAM GROUND pin (25) ±0.4 volts, the output waveform will lead the reference by 90°. A +2.4 volts or open will inhibit this phase shift. All program voltages are referenced to PROGRAM GROUND.
30	AUTO RANGE/RANGE SELECT PROGRAM – The switch must be in the RANGE SELECT position to be programmable. An open or +2.4 volts places the system in the RANGE SELECT mode. A ground ±0.4 volts selects the AUTO RANGE mode. All program voltages are referenced to PROGRAM GROUND.
31.	+180° PROGRAM – Discrete phase shift program, If this pin is grounded to PROGRAM GROUND pin (25) ±0.4 volts, the output waveform will lead the reference by 180°. A +2.4 volts or open will inhibit this phase shift. All program voltages are referenced to PROGRAM GROUND.
32	LOOP TIME CONSTANT – This allows the filter Loop Time Constant to be changed. When a PROGRAM GROUND pin (25) ±0.4 volts is applied, the low frequency time constant will be selected. An open or +2.4 volts will select the higher frequency range. The Loop Time Constant programming should be in the low frequency mode when phase locking frequencies 600 Hz and below. The high frequency Time Constant should be selected for phase locking frequencies higher than 600 Hz.
33	CONTINUOUS PHASE SHIFT CONTROL – A dc voltage may be applied to this pin to control the phase shift with a sensitivity of 100 mV/degree. This voltage must be referenced to CIRCUIT GROUND pin (18). The input impedance is 100 kΩ.
34	PHASE LOCK PROGRAM – When the PHASE LOCK/OPEN LOOP pushbuttons on the front panel is selected in the OPEN LOOP mode this pin may be used to program this operating mode. A PROGRAM GROUND pin (25) ±0.4 volts will select the PHASE LOCK mode. An open or +2.4 volts will select the OPEN LOOP mode. Voltages are referenced to PROGRAM GROUND pin (25).

TABLE 2-3 MODEL 755-S-206 PHASE PROGRAM CONNECTOR PIN LOCATION



Pin No. Description

4 RECORDER OUTPUT — A dc voltage proportional to the phase reading is available between this pin and CIRCUIT GROUND pin (18). −10 mV/degree from 1 kΩ impedance.

5 CIRCUIT GROUND — Reference for RECORDER OUTPUT pin (4) and CONTINUOUS PHASE SHIFT CONTROL pin (16). The CIRCUIT GROUND is isolated from PROGRAM GROUND.

6 PROGRAM GROUND — Is isolated from CIRCUIT GROUND pin (5) circuit common and is tied to power ground. All program voltages are referenced to PROGRAM GROUND.

7 −30° PROGRAM — Discrete phase shift program. If this pin is grounded to PROGRAM GROUND pin (6) ±0.4 volts, the output waveform will lag the reference by 30°. A +2.4 volts or open will inhibit this phase shift. All program voltages are referenced to PROGRAM GROUND.

Pin No. Description

8 −90° PROGRAM — Discrete phase shift program. If this pin is grounded to PROGRAM GROUND pin (6) ±0.4 volts, the output waveform will lag the reference by 90°. A +2.4 volts or open will inhibit this phase shift. All program voltages are referenced to PROGRAM GROUND.

9 +30° PROGRAM — Discrete phase shift program. If this pin is grounded to PROGRAM GROUND pin (6) ±0.4 volts, the output waveform will lead the reference by 30°. A +2.4 volts or open will inhibit this phase shift. All program voltages are referenced to PROGRAM GROUND.

10 +90° PROGRAM — Discrete phase shift program. If this pin is grounded to PROGRAM GROUND pin (6) ±0.4 volts, the output waveform will lead the reference by 90°. A +2.4 volts or open will inhibit this phase shift. All program voltages are referenced to PROGRAM GROUND.

Pin No.	Description
13	AUTO RANGE/RANGE SELECT PROGRAM – The switch must be in the RANGE SELECT position to be programmable. An open or +2.4 volts places the system in the RANGE SELECT mode. A ground ±0.4 volts selects the AUTO RANGE mode. All program voltages are referenced to PROGRAM GROUND.
14	+180° PROGRAM – Discrete phase shift program. If this pin is grounded to PROGRAM GROUND pin (6) ±0.4 volts, the output waveform will lead the reference by 180°. A +.24 volts or open will inhibit this phase shift. All program voltages are referenced to PROGRAM GROUND.
15	LOOP TIME CONSTANT – This allows the filter Loop Time Constant to be changed. When a PROGRAM GROUND pin (6) ±0.4 volts is applied, the low frequency time constant will be selected. An open or +2.4 volts will select the higher frequency range. The Loop Time Constant programming should be in the low frequency mode when the 755 is used for phase measurement and when phase locking frequencies 600 Hz and below. The high frequency Time Constant should be selected for phase locking frequencies higher than 600 Hz.
16	CONTINUOUS PHASE SHIFT CONTROL – A dc voltage may be applied to this pin to control the phase shift with a sensitivity of 100 mV/degree. This voltage must be referenced to CIRCUIT GROUND pin (5). The input impedance is 100 kΩ.
17	PHASE LOCK PROGRAM – When the PHASE LOCK/OPEN LOOP pushbuttons on the front panel is selected in the OPEN LOOP mode this pin may be used to program this operating mode. A PROGRAM GROUND pin (6) ±0.4 volts will select the PHASE LOCK mode. An open or +2.4 volts will select the OPEN LOOP mode. Voltages are referenced to PROGRAM GROUND pin (6).

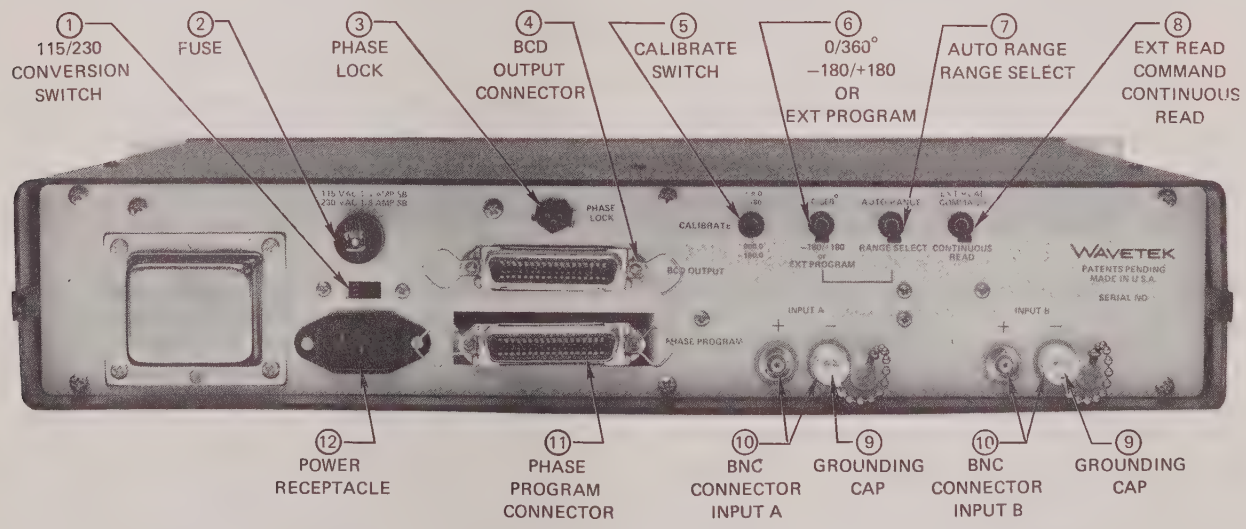


Figure 2-1. Operating Controls

2.3 OPERATING CONTROLS

The operating controls and electrical connections for the Model 755 rear panel are shown in Figure 2-1. The listing below discusses each control and its function.

1. **115/230 CONVERSION SWITCH** – Converts the power transformer to be used with either 115 Vac or 230 Vac.
2. **FUSE** – ½ amp to 115 Vac, ¼ amp for 230 Vac.
3. **PHASE LOCK** – Connection for controlling the 157-S-140 when used in a phase locked operation.
4. **BCD OUTPUT CONNECTOR** – A digital output representing the phase angle between the two inputs. See Table 2-2 for input and output programming connections and associated interface information.

5. **CALIBRATE SWITCH** – Used for quick check of phase detector calibration and digital offset.

6. **0/360 – 180/+180 or EXT PROGRAM** – This switch allows manual selection of phase range limits. When in the 0/360 position the Model 755 is in the 0° to 360° phase range. When in the –180/+180 or EXT PROGRAM position the Model 755 is in the –180° to +180° phase range or externally programmable, which allows the phase range to be changed by an external signal applied to the appropriate pin on the BCD connector (See Table 2-2).

7. **AUTO RANGE/RANGE SELECT** – In the AUTO RANGE position the Model 755 automatically changes its phase range as needed for a specific phase angle measurement. When in the AUTO RANGE mode the 0/360 –180/+180 range switch is deactivated. In the RANGE SELECT position the operator has the capability of manually selecting the range he desires.

8. **EXT READ COMMAND/CONTINUOUS READ** – In the EXT READ COMMAND position, an external read command pulse must be received at the BCD connector (See Table 2-2); which will allow the system to update its reading and give one print command. The instrument will hold the phase reading until another external print command is received, at which time it will update the reading and give another print command, when the data is available, on the BCD OUTPUT connector and the front panel display. In the CONTINUOUS READ position the instrument will continually update its reading every second and give a print out command upon each updating.

9. **GROUNDING CAPS** – Is a special BNC cap that shorts the connector to circuit ground.

10. **BNC CONNECTOR** – Input connectors for the signal source to be measured.

11. **PHASE PROGRAM CONNECTOR** – Accessory plug, providing phase programming connection to the 755 and is parallel with the programming inputs on the BCD OUTPUT Connector.

12 **POWER RECEPTACLE** – Connection for detachable line cord.

FRONT PANEL (not shown)

POWER – On/Off switch for power.

PHASE LOCK – When depressed places the 755-S-206 in the phase lock mode.

OPEN LOOP – When depressed, places the 755-S-206 in the phase measurement mode and isolates the phase lock control from the 157-S-140, allows both the 157-S-140 and the 755-S-206 to be used separately. When depressed the 755 phase lock mode may be remotely programmed as specified on the BCD OUTPUT connector description. (See Table 2-2).

2.4 PRELIMINARY CHECKS

This paragraph outlines a quick bench checkout procedure for determining proper operation of the instrument. Field calibration and checkout instructions are given in Section 4 for determining if the unit is within all electeical specifications. No special test equipment is required to perform the checkout of the instrument as outlined below:

1. Connect the line cord to the instrument and the line supply, depress POWER pushbutton, and allow a 30 minute warmup period.

2. Position the rear panel switches as follows:
   0/360 –180/+180 or EXT PROGRAM to 0/360
   AUTO RANGE/RANGE SELECT to RANGE SELECT
   EXT READ COMMAND/CONTINUOUS READ to CONTINUOUS READ

3. Hold the CALIBRATE switch in the +360.0/+180.0 position. The readout should display "+360.0" ±000.2°.

4. Hold the CALIBRATE switch in the 000.0/–180.0 position. The readout should display "000.0" ±000.2°.

5. Change 0/360 –180/+180 or EXT PROGRAM switch to the –180/+180 position, and hold the CALIBRATE switch in the +360.0/+180.0 position. The readout should display "+180.0" ±000.2°.

6. Hold the CALIBRATE switch in the 000.0/–180.0 position. The readout display should read "–180.0", ±000.2°.

If, after sufficient warmup, the proper readings are not observed, refer to the Calibration Instructions given in Section 4 paragraph 4.2 of this manual.

2.5 OPERATION PROCEDURE

2.5.1 Phase Angle Measurement

To measure the phase angle between any two ac signals within the specified frequency and amplitude ranges, proceed as follows:

1. Set the EXT READ COMMAND/CONTINUOUS READ switch in the CONTINUOUS READ position.

2. Set the AUTO RANGE/RANGE SELECT switch in the AUTO RANGE position.

NOTE

The 0/360 —180/+180 switch is deactivated in this mode.

3. Program the appropriate amplitude range (with no programming the instrument is in the least sensitive range .3 - 300 V range.)

4. For all phase measurements, program the low frequency constant by connecting pin (32) to pin (25) Program Ground on BCD OUTPUT connector.

5. Connect one ac signal to INPUT A and the other signal to INPUT B.

N O T I C E

If single-ended ac inputs are used, the grounding cap must be connected to the unused input BNC. If differential ac inputs are used, the grounding caps must be removed and the input signal must be connected between the positive and negative (+ and —) BNC.

If the readout jumps or scatters occasionally with low input amplitude and/or frequency, it is probably caused by noise spikes riding on the input signal or a high signal to noise ratio. To eliminate or reduce this effect, connect a 0.1μF capacitor (or matched filters) across input terminals.

N O T I C E

6. Read phase angle (phase difference) directly on digital display. If the readout polarity is positive, INPUT B leads INPUT A by the measured number of degrees. If the readout polarity is negative, INPUT B lags INPUT A by the measured amount.

7. The BCD OUTPUT provides the same data, electronically, for use as a control signal or for general recording applications.

8. For system operation, the Phase Range, Amplitude Range, and Range Calibrate pins may be externally programmed and the External Read Command feature may be utilized as specified in the BCD OUTPUT connector (See Table 2-2).

2.5.2 Phase Lock Operation

For Phase Lock operation, set up the 755-S-206 as shown in Figure 2-2 and set the controls as follows:

FRONT PANEL

1. POWER pushbutton should be depressed.

2. PHASE LOCK pushbutton should be depressed.

REAR PANEL

3. EXT READ COMMAND/CONTINUOUS READ may be set in either position depending on the desired mode of operation (see description page 2-6).

4. AUTO RANGE/RANGE SELECT set in the RANGE SELECT mode.

5. 0/360 —180/+180 or EXT PROGRAM may be manually selected or programmed to the position required for desired phase shift as follows:

   ±180° Range — Frequency capture at zero degrees then phase shift discrete ±30°, ±90° or analog ±12 V max. (±120° relative to zero degrees max.)

   0/360° Range — Frequency capture at 180 degrees then phase shift discrete ±30°, ±90° or analog ±12 V max. (±120° relative to 180 degrees max.)

NOTE

The Loop Time Constant programming should be in the low frequency mode when locking frequencies 600 Hz and below. The high frequency Time Constant should be selected for frequencies higher than 600 Hz. Program as specified. (See BCD OUTPUT connector Table 2-2).

Capture phase lock in center of selected phase range, after locking has been achieved, discrete phase shifts may be programmed within the range limits without recapturing.

NOTE

If 755 is not phase locking, check interconnections for proper channel input to 755, controlled frequency to Channel A, reference frequency to Channel B, phase lock connector to 157, and that system is in phase locked mode. (See Figure 2-2).

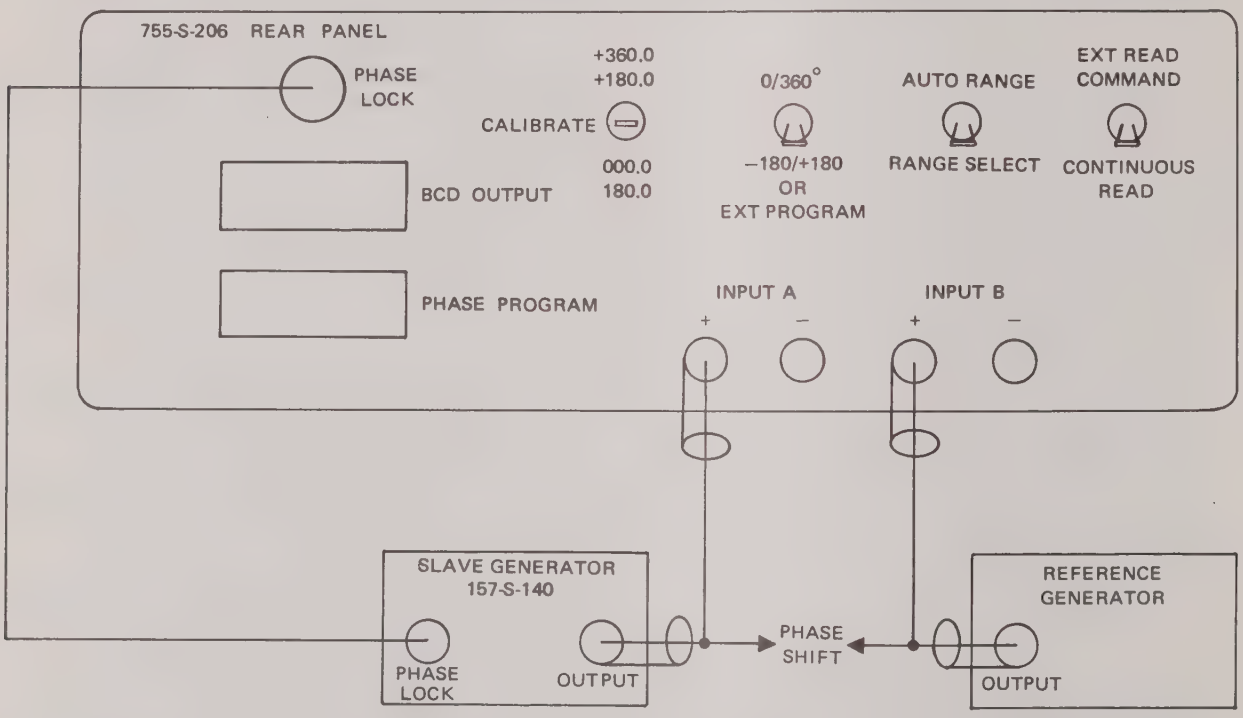


Figure 2-2. Phase Lock Set Up

SECTION 3
CIRCUIT DESCRIPTION

3.1 SIMPLIFIED BLOCK DIAGRAM

As shown in Figure 3-1, the Model 755 Programmable Phase Meter consists of two similar input channels (only the A channel has the 0/360 −180/+180 selector switch) and a common output channel. Paragraph 3.2 provides further descriptions of the functions of each basic circuit comprising this instrument. This paragraph describes, briefly, the major circuit elements and their relationship to one another.

The Frequency Compensated Attenuator in each input channel is used to reduce high amplitude inputs to a level suitable for the remaining circuitry.

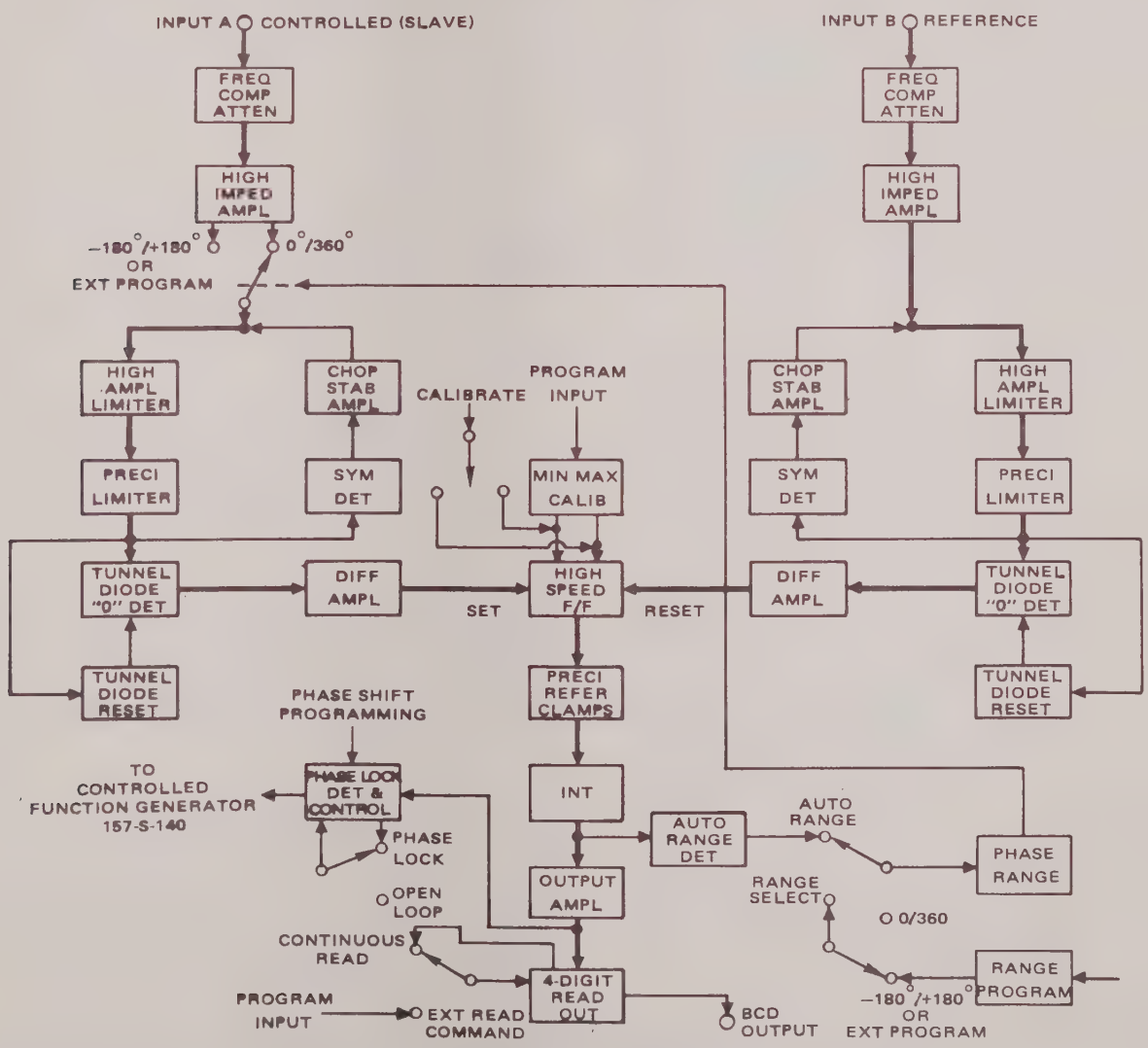


Figure 3-1. Simplified Block Diagram

The selected input signal is applied, through a High Impedance Attenuator, to a High Impedance Amplifier stage. In the A channel, the 0/360 −180/+180 or EXT PROGRAM switch select the appropriate phase out of the differential amplifier. The B channel does not employ a 180° phase shifter, as only one is needed in the instrument. Another function of the High Impedance Amplifier is to isolate the plus and minus inputs and provide high common mode rejection.

Next, the signal is high-amplitude-limited to prevent overdriving in the Precision Limiter stage. The Precision Limiter is a nonlinear feedback, wideband amplifier which limits the input signal at ±100 μV. The limited output signal is applied to a Symmetry Detector which integrates the waveform and produces a dc voltage that is proportional to the symmetry of the clipped waveform. This dc output represents an error in the zero-crossing system or an error due to the distortion of the input signal. The dc level is amplified and inverted in a Chopper Stabilized Amplifier and summed at the input to the first limiter stage. The closed-loop circuitry provides long-term, stable phase detection and automatically balances the limiters to correct for drift or offset voltages in the system due to temperature variations or component aging. Errors due to even-harmonic distortion are essentially eliminated by this self-balancing zero-crossing technique.

Following the limiters, the waveform zero-crossing is detected in a wideband Tunnel Diode Zero Detector. The Tunnel Diode Reset supplies the reset signal to the detector and provides system noise immunity. The detected zero-crossing output is then applied to the High Speed Flip-Flop through a Differentiating Amplifier. The output of Channel A is applied to the "set" input, and the output of Channel B is applied to the "reset" input of the flip-flop.

The flip-flop output is applied to a Precision Reference Clamp stage which provides a signal having an amplitude defined by the reference voltage and a duty cycle proportional to the phase difference between the two input signals. This output is integrated into a dc voltage proportional to the phase difference and is applied to the Output Amplifier for full scale and zero adjustment, before being applied to the digital display readout and output connectors.

The Range Maximum and/or Minimum calibrate programmable capability allows the instrument to select the maximum or minimum range, of the range selected, for presentation on the digital readout.

The Auto Ranging is only in the circuit when the AUTO RANGE switch is closed, through which the Auto Range Detector indicates to the Phase Range when either of the range extremes are approached. The Phase Range automatically changes to the appropriate phase range. During the transition, the digital readout is inhibited so that an erroneous reading is not presented to the BCD output during the change. The automatic ranging cycle takes approximately two seconds.

The inputs and outputs are isolated from circuit ground by means of the input isolation and the isolation board.

The phase lock circuitry is used to phase lock a controlled frequency generator (157-S-140) to an external frequency source.

3.2 FUNCTIONAL BLOCK DIAGRAM ANALYSIS

As each functional circuit is described, refer to the appropriate block diagram and, if necessary, the appropriate portions of the schematic diagrams at the rear of this manual.

3.2.1 Zero Crossing Circuit

Both input channels employ similar Zero Crossing Circuits; the only difference being the RANGE switch in Channel A. In view of this, only the functions of Channel A are described, realizing that there are counterparts in Channel B. Figure 3-2 is a functional block diagram of the Zero Crossing Circuit, Figure 3-3 shows key waveforms within this circuit.

The input signal is passed through the amplitude programmable frequency compensated attenuator before being applied to Q1-Q2. The plus and minus inputs are symmetrically attenuated in the ac/dc attenuator which is adjusted for a flat frequency response by trimmer capacitors C1 and C5.

The input source currents for the High Impedance Differential Amplifier stage are balanced by trimmer adjust R187 to yield best common mode rejection. The output of Q1-Q2 is applied, through the selected RANGE switch, to either the positive or the negative input of Input Amplifier IC1.

Trimmer capacitors C10 and C11 adjust the phase shift of the negative and positive inputs to IC1 to match those of IC4 in Channel B for best high frequency performance. IC1 provides either a 180° or a 0° phase shift, depending on the setting of the RANGE selector switches. With either range the gain of IC1 is unity, and its output is applied to the summing junction at the gate of Q3. FET Q3 and transistor Q4 provide a high input impedance to the summing point, as well as temperature compensation. The output from Q3-Q4 is applied to the symmetrical Amplitude Limiter CR1-CR4. R21 is used to balance this four-diode limiter.

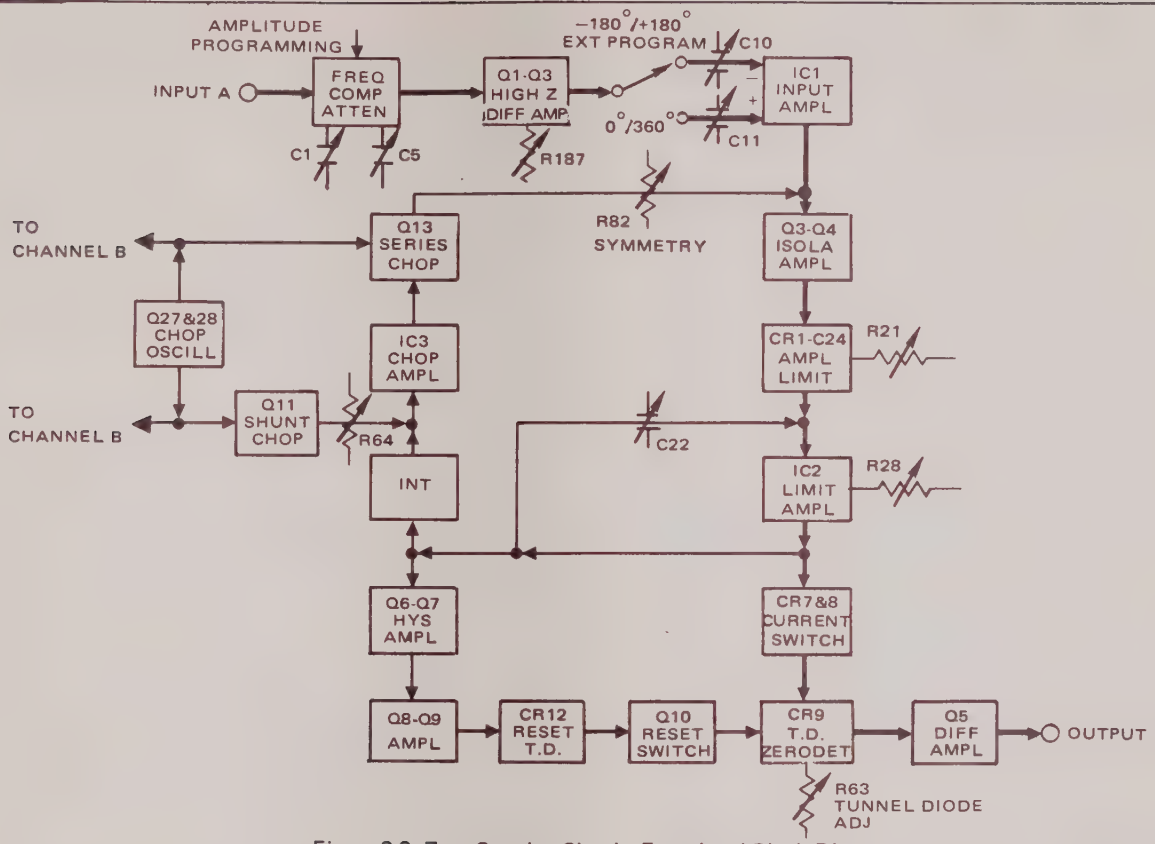
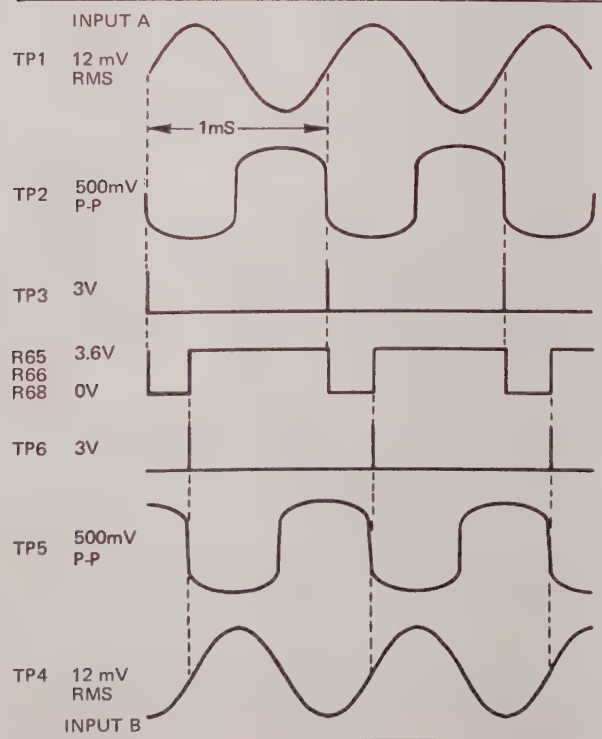


Figure 3-2. Zero Crossing Circuit, Functional Block Diagram



NOTES

PHASE RANGE 0/360°

INPUTS 10 mV RMS

CHANNEL B LAGS BY 90°

Figure 3-3.
Timing Diagram, Zero Crossing, and Logic Circuit

The output from CR1-CR4 is coupled to Precision Limiting Amplifier IC2, a 50 MHz amplifier with nonlinear feedback. R28 is a dc balance adjustment, C22 is a phase matching trimmer. The output of IC2 is a clipped waveform having an amplified volts/second relationship at the zero crossing of the input waveform.

For high accuracy, the output of the final limiting amplifier of a zero crossing system must be symmetrical for a sine wave input. To ensure this, the output waveshape must be sampled periodically and the result fed back to the input of the first limiter to correct any unbalance or dissymmetry. The Integrator (comprised of R37-R40 and C26 and C30) supplies a dc voltage proportional to the symmetry of the output of IC2 to the input of Chopper Amplifier IC3. Shunt Chopper Q11 converts the dc output of the Integrator to an ac signal. R64 is the chopper balance adjust.

This ac signal is then amplified in IC3, and the output is demodulated in Series Chopper Q13. The voltage developed across capacitor C59 is an amplified error signal proportional to the nonsymmetry of the output of IC2. This error signal is applied, through R23, to the summing point at the gate of Q3. R82 is a symmetry adjustment which controls the amount of error signal in the feedback loop. This chopper-stabilized symmetry-detection system also eliminates the effects of even harmonic distortion with the limits of the chopper loop.

The symmetrical output of IC2 is then applied to Current Switch CR7-CR8 which supplies a small amount of current, at the actual zero crossing point, to trigger Tunnel Diode Zero Detector CR9. Tunnel Diode Adjust R63 sets the firing point of CR9 to be at the zero crossing point.

Differentiating Amplifier Q5 then supplies a pulse output which occurs at the true zero crossing point of the input waveform.

The reset circuitry for CR9 consists of transistors Q6 through Q10. Hysteresis Amplifier Q6-Q7 amplifies the output of IC2 and provides the necessary hysteresis to prevent double triggering. The output from Q6-Q7 is applied, through Amplifier Q8-Q9, to reset Tunnel Diode CR12. When CR12 fires, the resultant waveform is differentiated and drives Reset Switch Q10 to saturation which, in turn, resets the Tunnel Diode Zero Detector CR9 to its original state.

Chopper Oscillator Q27-Q28 is the circuitry common to both channels of the Zero Crossing Circuit. This oscillator supplies the chopper pulse which drives the gates of field-effect-transistors Q11 and Q13 at the proper sample rate.

3.2.2 Logic Circuit

The Logic Circuit converts the pulse information generated by the Zero Crossing Circuit into a precision, linear dc voltage whose value is a direct function of the phase difference between inputs A and B.

The two pulses generated by the Zero Crossing Circuit are applied to the inputs of a fast rise and fall time Set-Reset Toggle IC4. This stage is a dual transistor gate connected as an RS toggle with hot carrier diodes CR13 and CR14 providing nonsaturated, high speed operation. This stage converts the pulse information into a rectangular waveform that drives Saturated Switch Q18-Q19.

When the CALIBRATE switch is actuated, it inhibits either the "A" or "B" input from the Zero Crossing Circuit. With one input inhibited, the Set-Reset Toggle IC4 will go to a single state and remain. One state of IC4 corresponds to 0°, the other state corresponds to 360°. Therefore, when CALIBRATE switch SW3 is actuated, all dc calibrations may be checked.

Q18-Q19 operates as a pair of saturated switches between ground and a precision +3.6 Vdc. The resulting output, at the junction of R65 and R66, is integrated in Integrator R68/C24 and then filtered by an active Unity Gain Filter comprised of IC5, R69, R70, C25, and C26. Q20 functions as an Emitter Follower input to the Unity Gain Filter.

The integrated and filtered signal, representing the phase angle between INPUT A and INPUT B, is then conditioned in the Unity Gain Amplifier IC6. The final dc voltage out of IC6 has a −10 mV/degree relationship to the measured phase angle, and is provided (at J8) as an output as well as the input to the Digital Display Circuit.

RANGE calibration is accomplished by four potentiometers at the rear of the unit. When the 0°/360° RANGE is selected, the +360.0 and 000.0 limits may be calibrated using R79 and R81 respectively. When the −180°/+180° RANGE is selected, the +180.0 and the −180.0 limits may be calibrated using R22 and R84 respectively.

The reference voltage at the integrator input is the same voltage used as the voltmeter reference. The result is a ratio measurement that is independent of power supply drift.

3.2.3 Auto Range Circuit

Refer to the Auto Range Board Schematic at the rear of this manual when reading the following circuit description.

The filtered output of the Logic and Power Supply Board is applied to pin 13 of the Auto Range Board. The filter

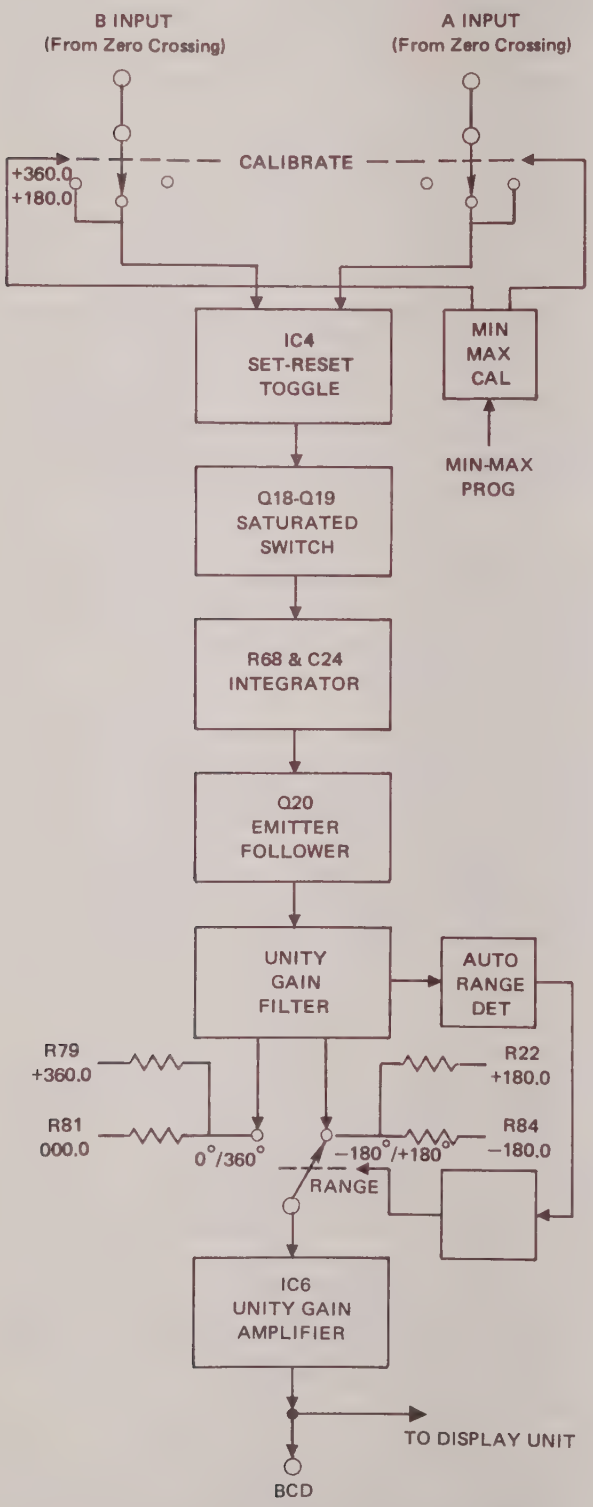


Figure 3-4. Logic Circuit, Functional Block Diagram

output is a dc voltage proportional to the phase shift between the inputs to the phase meter. This dc voltage is always between zero and 3.6 volts for 360 degrees. This dc voltage is then applied, through R13 and R14 to a dual comparator. The comparator has two reference voltages against which it compares the filter output. One is a positive reference voltage determined by R10 and R12, adjustable between zero and 1 volt approximately. This is the low level set point.

The high level set point is determined by R16 and R17, and can be set between 3 and 3.6 volts approximately. When the filter output approaches and equals either one of the set limit voltages, the output of the comparator (at pin 9 on Auto Range Board) makes a negative transition. This negative transition is coupled through C3 to toggle the JK flip-flop IC2 to the opposite state. The change of state of IC2 provides a signal at pin 7 which drives the range switch transistor Q2 and, in turn, drives the range change relays to the opposite range.

At the same time the negative transition toggles IC2, this negative transition is also applied to Q5 through R25. This inverts the pulse to a positive going pulse which triggers the single shot, IC3. IC3 has a two-second time constant such that when it is triggered pin 7 of this single shot drives Q4, through R23, and holds it in the conducting state. This action holds the junction of C3 and R24 to zero so that IC2 cannot make another transition until the range has been changed and the filter output (pin 13 of this board) has reached its steady state condition.

The relays for the auto ranging circuitry (K5, K6, K7, and K8) change the input phase shift of Channel A to add a 180 degree phase shift for the 0 to 360 degree mode. It also adds an opposing dc bias voltage in the phase detector circuitry so that the digital readout is compensated for the phase shift added to the input.

The programmable amplitude ranges are also located on the Auto Range Board. Q1 and Q3 are the relay drivers associated with the relays for Channel A and Channel B amplitude programming respectively. Relays K1, K2, K3, K4, K9, K10, K11 and K12 program the attenuators for Channel A and Channel B.

3.2.4 Minimum Maximum Calibrate Circuit

Refer to the Phase Lock Board Schematic at the rear of this manual when reading the following circuit description.

The two transistors Q16 and Q17 are relay drive transistors which when energized, actuate K12 and K13 relays. When pin 21, of the BCD output connector is grounded, transistor Q17 is energized; which is the closure on K13 relay. This

places the system in the minimum calibration range mode displaying 000.0 or −180.0 on the front panel digital output and is also available at the BCD output connector. If pin 22, of the BCD output connector is grounded transistor Q16 is energized which provides the closure on relay K12. This places the system in the maximum calibration range mode.

This allows the maximum reading of the range selected, 360.0 or +180.0, to be presented on the front panel digital display and the BCD output connector.

3.2.5 Digital Display Circuits

The Digital Display Circuit is a four-digit, automatic-polarity-indicating, dual-slope-integrating, digital voltmeter (DVM). As this circuit is described, refer to the timing diagram (Figure 3-6) as well as the block diagram and schematic at the rear of this manual.

The −10 mV/degree dc output from the Logic Circuit is applied to the input of the Digital Display Circuit. This input is switched into an integrator for a precise time interval, causing the integrator to "ramp" to some voltage. At the end of the input time interval, a reference voltage is switched into the integrator causing it to ramp back to zero. The time between the start of the reference ramp and the time the reference ramp passes through zero is converted to a timing pulse by logic circuitry. The width of this pulse is directly related to the amplitude of the dc voltage input applied to the DVM, and thus, the phase relationship (phase angle) of INPUT A to INPUT B. This pulse is used to gate a counter so that, for each 1 mV of input voltage, one count is displayed, yielding .1° phase resolution on the digital readout.

The entire DVM is synchronized from a master clock, Oscillator IC7-Q17, which is scaled down in the four 10^N Decade Counters to provide the DVM time base. This time base controls the input to the Integrator, IC1, and sequences logic decisions used to generate the counter gating pulse.

The Integrator, IC1 and C2, has four inputs. The input voltage is switched in by Q1 and Q2. Depending on the input voltage polarity, either the +3.6 V reference is switched in by Q3 and Q4, or the −3.6 V reference is switched in by Q5 and Q6. Zero adjustment is made by R11 (ZERO OFFSET ADJ) which compensates for the input switch and integrator offset voltages.

It should be noted here that the +3.6 V used as the DVM reference is also the +3.6 V used to power the circuitry generating the dc output from the Logic Circuit. Thus, if the +3.6 V should change, there will be virtually no variation in the DVM output since a ratio relationship exists between the generating source and the measuring system.

The output of IC1 is detected in Comparator IC2 and the Amplifier comprised of Q8-Q10. IC3A and IC4A provide additional drive for the comparator input at zero, through Q7 and Q11, to prevent multiple comparator outputs. The amplified comparator output steers JK Flip-Flop IC5A which, upon receipt of the 10^{-3} 8 clock signal from IC5B, determines the polarity of the DVM input voltage. Once the polarity has been determined, either IC3B or IC4C changes state to switch in the appropriate reference voltage for ramping the integrator back to zero. As the reference voltage is switched in, IC3C is gated positive, producing the start of the output pulse. When the Integrator reaches zero, the Comparator changes state. This change in state causes IC3B or IC4C to gate IC3C negative, generating the end of the output pulse.

In the digital readout system, the analog board converts the dc output of the phase meter to a positive pulse whose width is proportional to the phase shift at the input to the instrument. This pulse is then applied to pin 4 of the Digital Readout Board.

The positive pulse is fed through R3 to the base of Q2, an inverter, causing the collector of Q2 to go negative for the same duration. The first negative transition of the pulse at the collector of Q2, coupled through C1, causes the output of IC2 to go positive. This positive output is applied to the reset pins of IC5, IC8, IC11, and IC14—the counter portion of the digital readout system. Thus, the negative transition of the pulse at the collector of Q2 causes a zero state to be set into the counter.

The clock input, a frequency of approximately 50 kHz, is applied through Q1 to pin 14 of IC5, the first decade of the decade counter stages. This frequency is then counted until a positive transition of Q2 is coupled through C2 causing IC2 to go negative. The single-shot configuration of IC2 provides a positive pulse at pin 8. This also drives pin 1 of IC1 to a positive condition which (if pins 8 and 11 of IC1 are in the reset condition) allows the pulse to get through to pin 3 of IC1 and pin 6 of IC1 to go negative. This action strobes the information from the clock decade counters into the latch circuits of IC4, IC7, IC10, and IC13, and also strobes the Print Command output circuit.

When the new information is updated into the quad latch circuitry, decoder drivers IC3, IC6, and IC9, and IC12 then decode the information and present it to the digital display tubes V1, V2, V3, and V4.

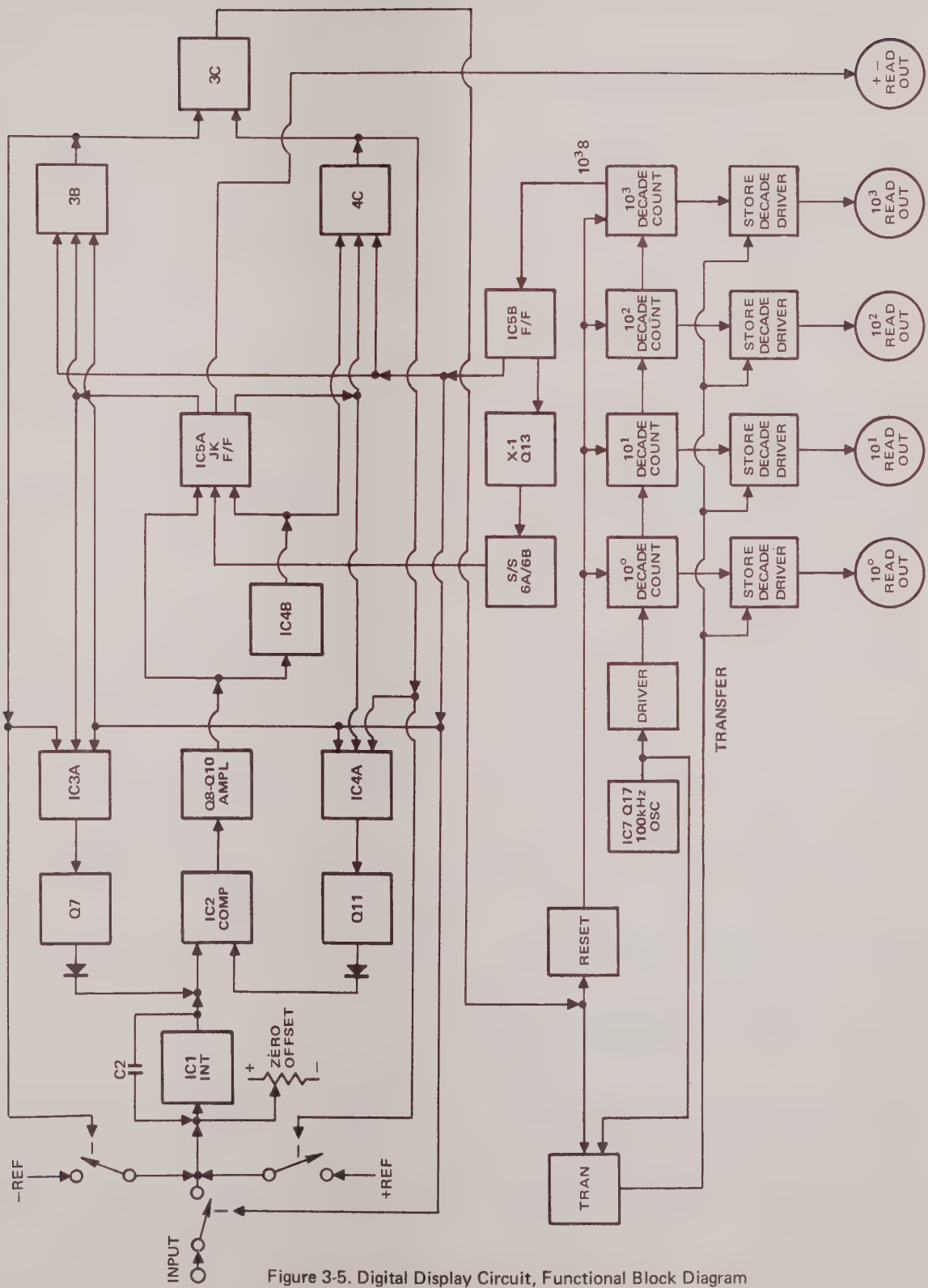


Figure 3-5. Digital Display Circuit, Functional Block Diagram

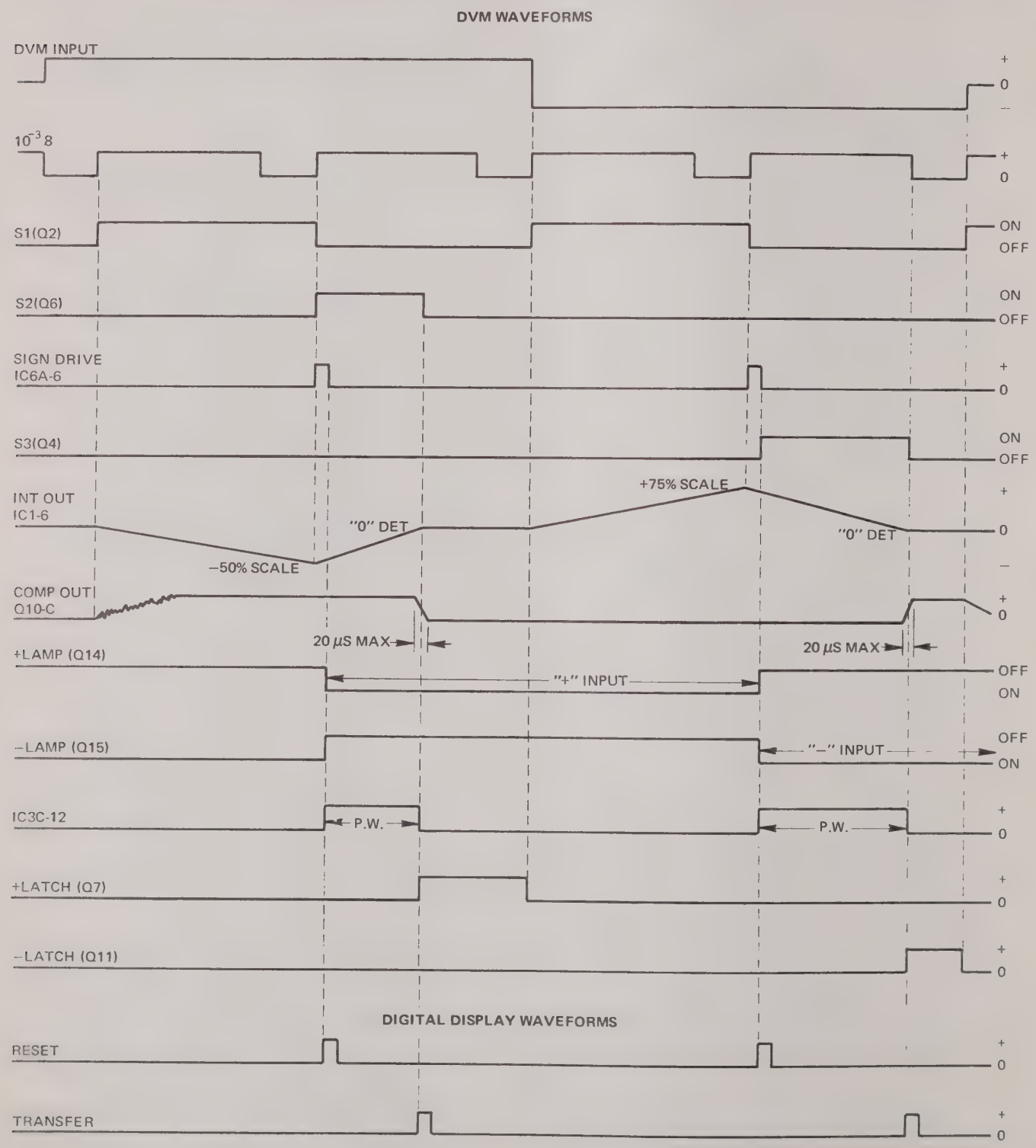


Figure 3-6. Digital Display Circuit, Timing Diagram

Another feature incorporated in the Digital Readout Board is the external read command. The external read command is an input through pin A6 which after passing through an isolation transformer T1 sets pin 11 of IC1 to a low condition when pin A6 is positive and when the rear panel switch is in the external read command position. When A6 is held positive, pin 11 is held at ground inhibiting the clock input at pin 2 of IC1. This action, in turn, inhibits the transfer command from the decade counters to the quad latch circuits. The print inhibit signal applied to pin 13 of IC2 inhibits the digital readout print command from external sources. In the normal Model 755 configuration, the auto range circuitry inhibits the digital readout during its transition period with this line.

Transistors Q3 and Q4 are the plus and minus sign drivers for the digital display tubes.

3.2.6 Phase Lock Circuit

Refer to phase lock board schematic when reading the circuit description of the Phase Lock Board. When the Model 755 is phase locking an external frequency to that of the Model 157 (phase lock mode), the following connections are made:

The external reference frequency is applied to the Channel B input of the Model 755.

The output of the Model 157 in the phase-lock loop (whose frequency is being controlled in relation to the external frequency) is applied to the Channel A input of the Model 755.

The rear panel PHASE LOCK connector of the Model 157 is connected to the rear panel PHASE LOCK connector of the Model 755.

When the output of the controlled Model 157 is programmed to equal the external reference frequency, and the PHASE LOCK button on the Model 755 is depressed or programmed, the two outputs will be equal in frequency and the phase angle between them will remain constant.

The following is an explanation of the circuitry needed to accomplish this phase locking:

The recorder output of the Model 755, after passing through R5 and R6, is applied to operational amplifier IC1. Pin 2 of IC1 is the summing node at which the external programmable discrete phase shifts are summed. The external summing phase shifts are +30 degrees, −30 degrees, +90 degrees, −90 degrees, 180 degrees, and a continuous analog phase shift control. Transistor Q1, which separates the summing node from the external phase shifts, is used in the automatic lock circuitry.

The discrete phase shifts are programmed through the phase program connector energizing transisters:

Q8 for the −30 degree phase programming, as set by R41 and R42.

Q9 for the −90 degree phase programming, as set by R43 and R44.

Q10 for the +30 degree phase programming, as set by R45 and R46.

Q11 for the +90 degree phase programming, as set by R47 and R48.

Q12 for the 180 degree phase programming, as set by R49 and R50.

R38 and R39 for the continuous phase programming.

The output of operational amplifier IC1 is then applied to a loop filter smoothing circuit comprised of R14, C12, and R16. Additional filtering is available for low frequency phase lock. Potentiometric amplifier IC2 amplifies this phase error voltage and applies it to R26.

NOTE

In a phase-lock system, it is possible for the controlled frequency to phase-lock to a harmonic of the reference frequency. In most cases, this is an undesireable quality.

If a harmonic error voltage is generated due to harmonic locking, the voltage fed to R26 will be either positive or negative, depending on whether it is the result of a harmonic lock or a sub-harmonic lock. Conditions of extreme frequency variation in reference to the external frequency, or temporary unlock due to external perturbations, can also cause an incorrect voltage at R26.

In any case, an erroneous voltage into R26 constitutes an unlock condition and, therefore, must be dealt with accordingly. The comparators, IC3 and IC4, compare the voltage at R26 to determine whether it is higher or lower than a set level established by positive set adjustment R54 or negative set adjustment R21.

If the voltage at R26 is more positive than zero, IC4 will change state causing Q5 to cease conducting, which pulls the FET series switch Q2 into a nonconducting state. When Q2 ceases conduction it essentially opens the phase-lock path and R30 allows the phase-lock control line to be pulled negative. This action brings the frequency of the controlled VCO (Model 157) closer to the reference frequency.

If the voltage at R26 is more negative than the set level established by R21, IC3 changes state turning off Q3. This, in turn, drives the gate of FET Q4 far negative; into the "pinch-off" region. This allows R33 to drive the control line more positive thereby bringing the controlled frequency closer to the reference frequency. When either condition occurs, the controlled frequency of the Model 157 is pulled closer and closer until it equals the reference frequency. At this point, the voltage at R26 reaches zero, the comparator amplifier returns to its normal state, Q2 and Q4 return to their normal on condition, and a closed loop feedback path is established for the phase-lock system.

Two RC paths are provided through the contacts of relays K10, K11 to the phase lock connector at the rear of the Model 755, and, in turn, the error amplifier circuitry of the Model 157 being frequency controlled. These two inputs to the Model 157 are offered as an option, with a connector on the rear of the Model 157 to mate with that on the rear of the Model 755. When both relay contacts are open, which is the case when the OPEN LOOP push-button on the front of the Model 755 is depressed, the Model 755 may be used as a standard phase meter and the Model 157 may be used as a standard waveform synthesizer.

Q6 on the phase lock board is a zener transistor used for the positive bias voltage for transistors Q5 and Q3. The isolated power supply, used in systems where isolated programming ground is required, is also located on this board. Transistor Q15 in conjunction with transformer T1 and the associated circuitry provides the power necessary to drive the program relays thereby isolating the program ground from the circuit ground.

3.2.7 Isolation Circuit

Refer to the Isolation Board Schematic at the rear of this manual when reading the following circuit description.

This option provides BCD data isolation by means of contact closured to the program ground which is isolated from the circuit ground. Relays K1 through K14 provide isolation for BCD outputs while K15 provides isolation for the + and – sign. Transformer T1 and T2 provide isolation for the external read command in and the print command output respectively. IC1 accepts the strobe command from the digital board and provides the necessary delay to allow all the relays to settle down before a print command is generated by the opening of Q3 collector.

3.2.8 DC Power Supplies

Regulated operating voltages for the Model 755 Phase Meter include +15 V, –15 V, +3.6 V, –3.6 V, +5 V, and +180 V. AC line voltage is connected through the line cord to the POWER switch on the front panel. A slo-blo fuse is installed on the line side of the switch, and a 115/230 power selector switch connects the primary winding of the power transformer for the appropriate line voltage.

AC voltage is coupled from the transformer secondary to the bridgerectifier CR1-CR4. Filtering is provided by C3 and C11. Q12 is operated as a Zener diode reference voltage for the –15 V supply. IC3 is a comparator differential amplifier. The Comparator drives a Darlington-connected Series Pass transistor pair, Q9 and Q11, used for added current gain. Q8 is also connected to operate as a Zener diode reference to provide a voltage level shift for the output of IC3. R36, –15 V ADJ, adjusts the minus input of IC3 with respect to the plus input which has a Zener voltage of approximately 7 volts. If the –15 V tries to increase due to a change in line voltage or load current, the collector of Q12 stays approximately at the same voltage. Thus, the minus input to IC3 becomes more positive than the plus input, and the IC3 output draws more current. The output moves less positive, and this change is coupled to the base of Q9 and Q11 through Q8, returning the supply to –15 volts.

IC1 is a Comparator Differential Amplifier in the +15 V supply. The plus input of IC1 is returned to ground through R9. Voltage Divider R7-R8, between the plus and minus 15-volt supplies, sets the minus input of IC1 precisely at ground. An increase in the –15 volts, due to line voltage variation or load current change, results in the minus input of IC1 moving positive, and the output of IC1 moving negative. This change is coupled to the bases of Q1 and Q2 through Q4. Q1 and Q2 form a Darlington-connected Series Pass pair for added current gain. The negative-going change returns the output to +15 volts.

Q3, in conjunction with R2 through R4, comprises a foldback current limiter for the +15 V regulator. Normally, the base of Q3 is turned off. Thus, the base of Q2 moves freely as the output from IC1 changes. When the +15 volt output is overloaded, heavy current flows through R2 and creates a potential drop across the resistor. When the potential drop overcomes the drop across R3, Q3 begins to conduct, starting to short the base of Q2 to the +15 volt output. In this condition, the output can be shorted indefinitely at a lower than maximum power dissipation of Q1. When the overload condition is removed from the +15 V output, the base of Q2 starts to rise. As the emitter of Q1 rises toward +15 volts, Voltage Divider R3-R4 has more effect on the base of Q3 and eventually turns Q3 off completely. When Q3 turns off, the normal condition is restored. Q10 with R28, R29, and R30, form a foldback current limiter for the –15 volt regulator.

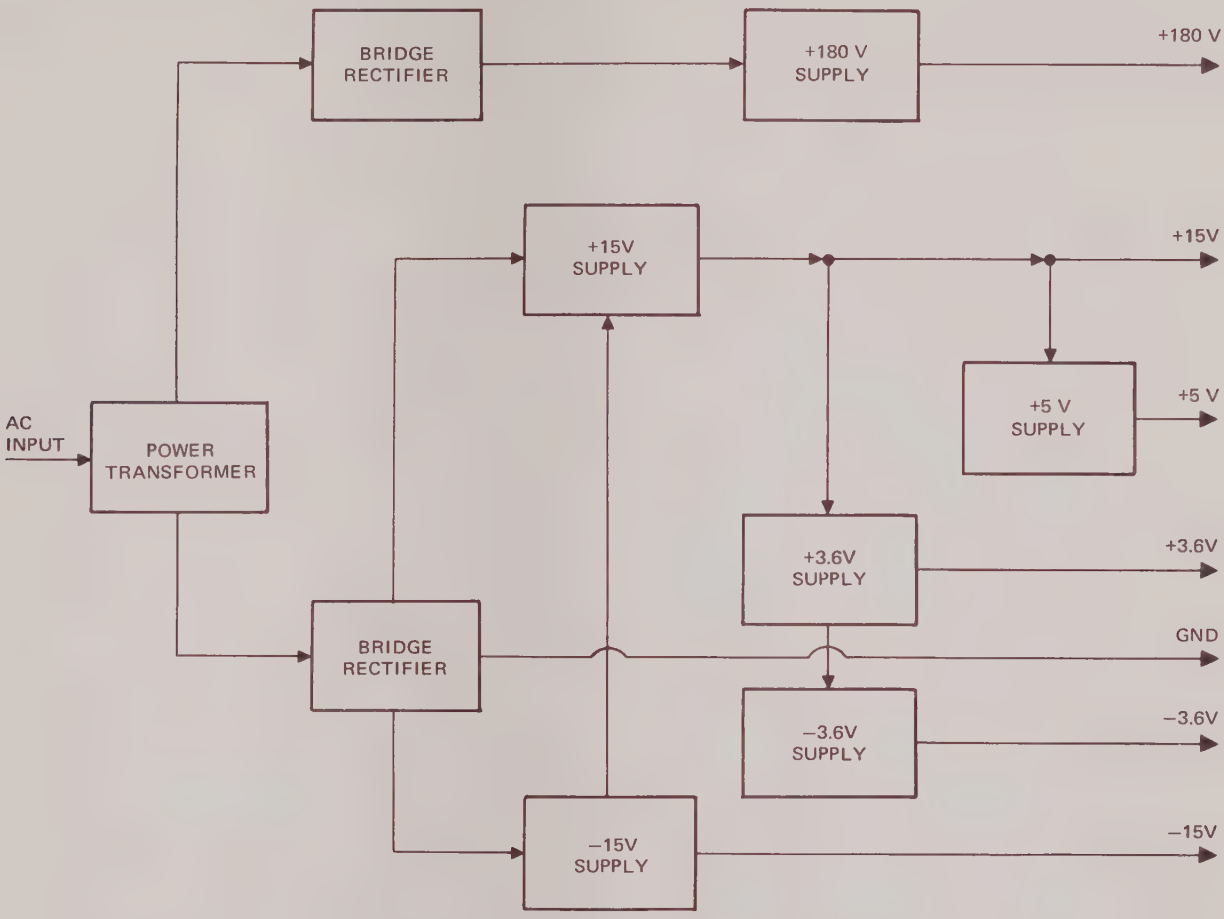


Figure 3-7. DC Power Supplies, Functional Block Diagram

The +3.6 volt supply is provided by Q5 and Q6 operating as a Comparator Differential Amplifier controlling the Series Pass transistor Q7. The error signal is obtained from the wiper of R20, in a Voltage Divider comprised of R18, R20, and R21 between +3.6 volts and −15 volts (the −15 volts here acts as a reference voltage) and R2 is used as the +3.6 volt adjustment.

The −3.6 volt supply is provided by IC2 operating as a Unity Gain Operational Amplifier with R22 providing gain control and the −3.6 volt adjustment.

For the +5 volt supply, ac voltage is coupled from the transformer secondary to Bridge Rectifier CR8-CR11. Filtering is provided by C14. Q14, Q15, and Q16 form a Comparator Differential Amplifier controlling Series Pass transistor Q13. The error signal is sensed directly on the +5 volts and is applied to the base of Q16. The Voltage Divider R38-R44, between +15 volts and ground, provides the reference voltage for the base of Q15. Q17, R40, R41, R42, and R43 form a foldback current limiter for the +5 volt regulator.

For the +180 volt supply, ac voltage is coupled from the transformer secondary to Rectifier CR12. Current limiting is provided by R48 and filtering is provided by C17. R49 is a bleeder resistor for C17, to prevent a sustained high voltage after power is turned off.

3.3 SUPPLEMENTAL CIRCUITS

There are no unique or supplemental circuits within the Model 755 to be separately described as "Supplemental Circuits". The preceding circuit descriptions adequately describe the complete circuitry of the Model 755 to the degree required by a competent technician.

SECTION 4
MAINTENANCE

4.1 ACCESS INSTRUCTIONS

Removal of the dust cover affords quick access to the majority of components within the unit. However, it may be necessary to remove the Digital Readout Assembly or the Zero Crossing Board in order to gain access to those components not exposed by removing the dust cover. Instructions for all three are given below.

4.1.1 Removing the Dust Cover

1. Unplug the power cord.
2. Unscrew three captive screws on top cover.
3. Remove top cover.
4. Follow same procedure for bottom cover removal.

4.1.2 Removing the Digital Readout Assembly

1. Remove the two Phillips screws on top of the Digital Readout Assembly closest to the front panel.
2. Remove the two Phillips screws holding the two bars extending from the assembly to the rear panel.
3. The assembly can now be removed and placed on a support resting on two side plates. The unit may be turned on and operated while in this stage of disassembly.
4. Disconnect the connector pins.

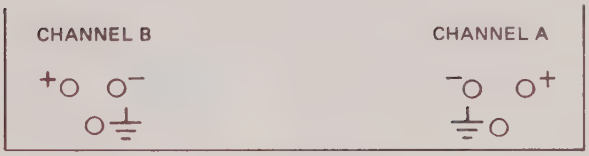
4.1.3 Removing the Zero Crossing Board

1. Remove bottom cover.
2. Place instrument on its top.
3. Remove the three bottom screws on both sides of the instrument holding the Zero Crossing Board to the side plates.
4. Disconnect the connector pins on front of instrument.

NOTE

The inputs are now available at the connector pins on the front of the Zero Crossing Board.

5. To replace the Zero Crossing Board, reverse the above procedure. When reconnecting the input connector pins, follow the diagram.



Component Side of Zero Crossing Board

4.2 CALIBRATION INSTRUCTIONS

This paragraph provides complete sequential calibration instructions for the Model 755 Phase Meter. The instructions are concise and are written for the experienced electronics technician or field engineer having a working knowledge of this type of instrumentation.

WAVETEK maintains a factory repair department for those customers not possessing the necessary test equipment or personnel to maintain this type of instrument. If an instrument is returned to the factory for calibration or repair, a detailed description of the specific problem should be attached. This will hasten turnaround time.

Test point and control locations necessary for calibration are given within this section unless a foldout illustration is required. In the latter instance, the foldout illustration will be found at the rear of the manual.

4.2.1 Recommended Test Equipment

The following test equipment (or equivalent) is recommended for this calibation procedure.

VCG/VCA Generator	Wavetek Model 136
Voltmeter	1 mV Resolution
Oscilloscope	with Dual Trace 10 mV Sensitivity Lissajous Capability

4.2.2 Preliminary Procedures

Before attempting to recalibrate this instrument, the user should read and understand the entire calibration procedure. The four major segments of this procedure should be performed in the sequence given, as should the steps within each segment.

1. Connect the Model 755 Phase Meter in the test set up illustrated in Figure 4-1 [A].
2. Set POWER switch to ON, set RANGE selector for 0°/360°, continuous read, range select.
3. Allow a 30-minute warmup period before attempting to calibrate this instrument.

4.2.3 Full Scale Calibration Procedure

4. With equipment connect as shown in Figure 4-1 [A]; hold CALIBRATE switch down (000.0/−180.0) and adjust (R81) for 000.0 plus or minus 1/2-count.

NOTE

One-half count (1/20th of a degree) can be determined by interpolation of alternate readings. If display alternates between ±000.0 and +000.1, the indication may be averaged to give +000.05. Careful adjustment should yield a display of ±000.0 (±.1) after equipment warmup.

5. Hold CALIBRATE switch up (+360.0/+180.0) and adjust (R79) for a display centered between +359.9 and +360.0.
6. Set RANGE selector for −180°/+180°.
7. Hold CALIBRATE switch down (000.0/−180.0) and adjust (R84) for a display centered between −179.9 and −180.0.
8. Hold CALIBRATE switch up (+360.0/+180.0) and adjust (R22) for a display centered between +179.9 and +180.0.
9. Repeat steps 4 through 8 for best indications. If all four calibrations are not within the specified limits, refer to the Logic Board Calibration Procedure given in paragraph 4.2.4.

4.2.4 Logic Board Calibration Procedure

10. Remove the top dust cover from the Model 755 Phase Meter following the procedures outlined in paragraphs 4.1.1 and 4.1.2.

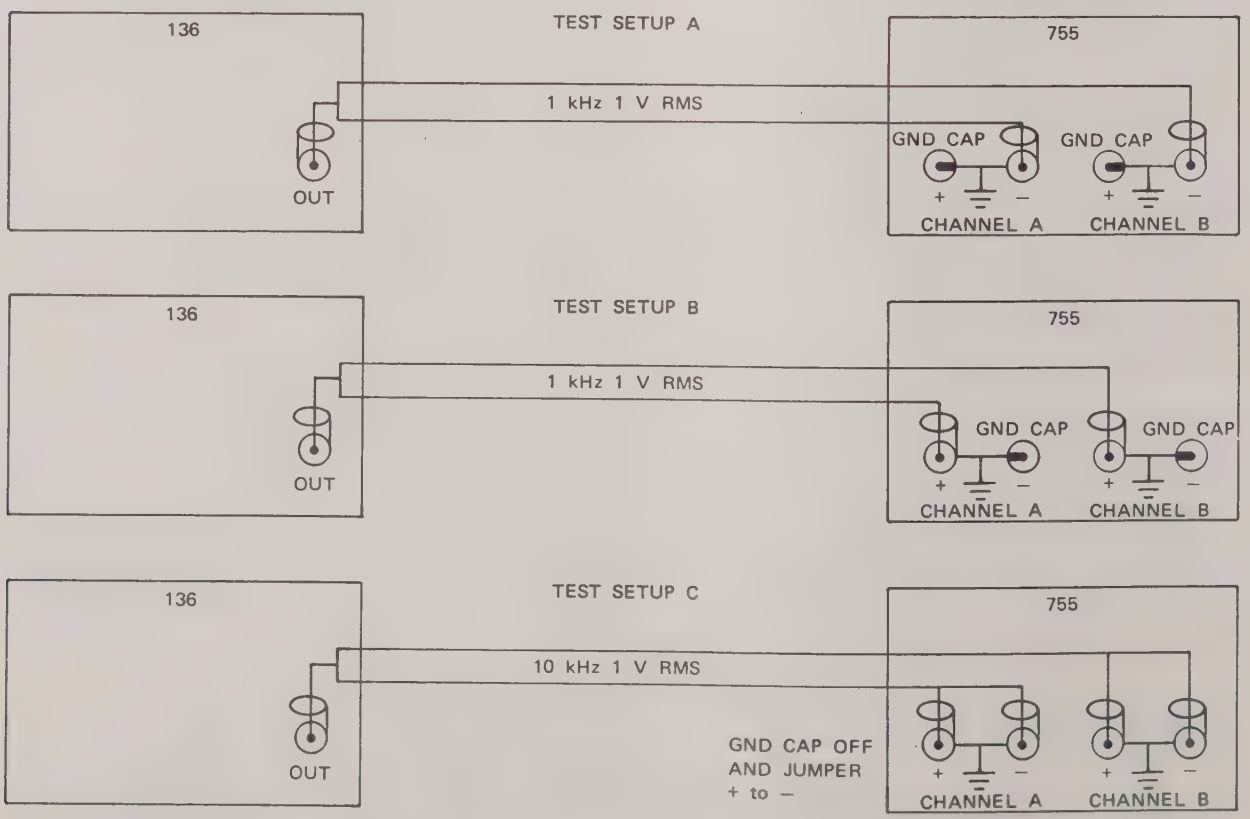


Figure 4-1. Calibration Set-up

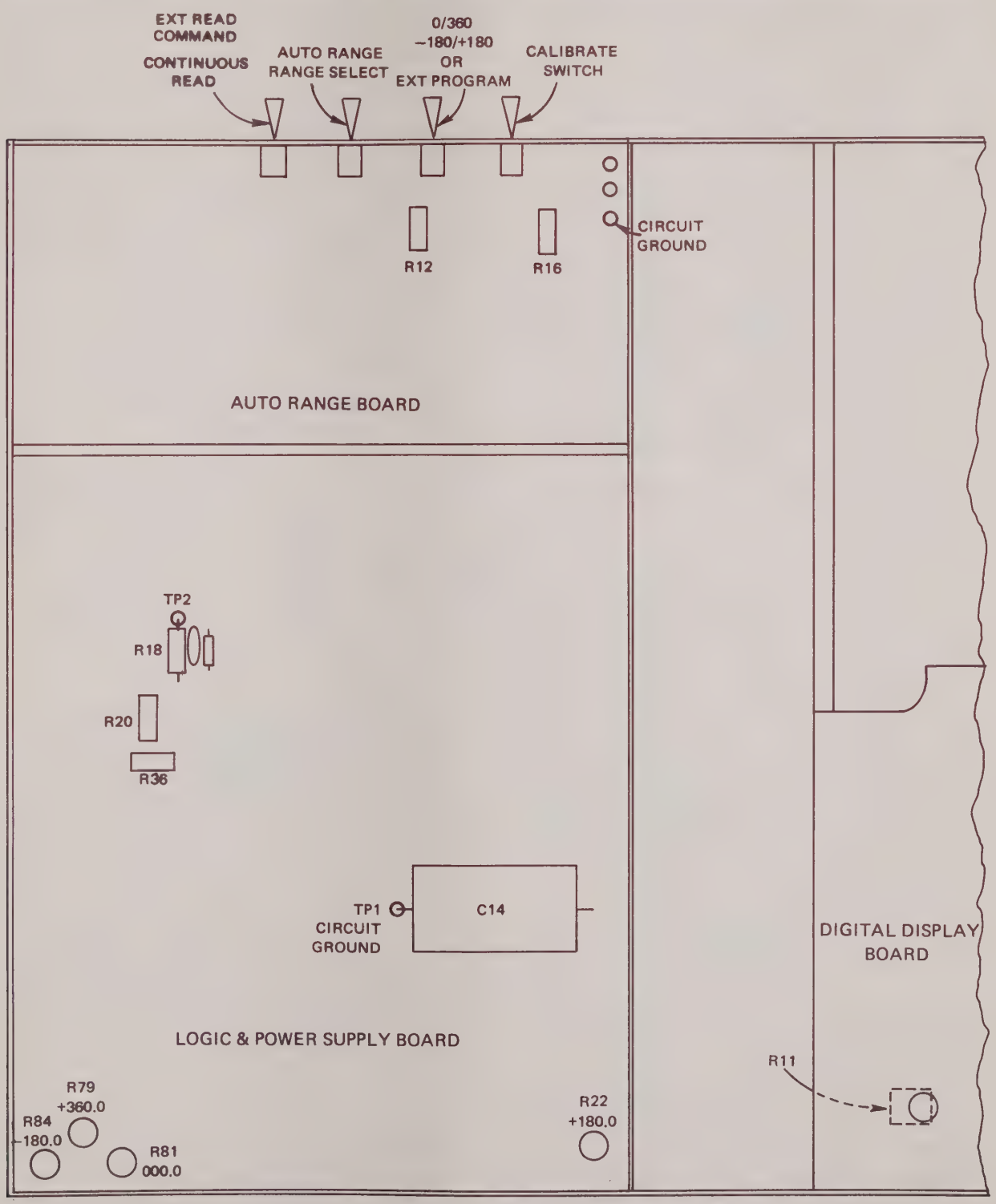


Figure 4-2. Calibration Locations on Logic, Auto Range and Digital Boards.

11. Connect the positive probe of the voltmeter to test point TP2, and the negative probe to TP1, of the Logic Board (Figure 4-2).
12. Set POWER switch to ON and allow a 30-minute warmup period.
13. Set RANGE selector to 0°/360°, and set (R20) to the center of its adjustable range.
14. Adjust (R36) to obtain +3.600 V (±2 mV between TP1 and TP2 (+3.6 V supply).
15. Connect the voltmeter to the Recorder Output at pin 17 on the BCD Output connector and circuit ground (TP1).
16. Hold CALIBRATE switch down (000.0/−180.0) and adjust (R81) for 0.000 V (±.3 mV) on the voltmeter.
17. Hold CALIBRATE switch down (000.0/−180.0) and adjust DIGITAL DISPLAY ZERO control R11 (accessible from the left side of the top printed circuit board of the Digital Display assembly) for a display of 000.0 plus or minus 1/2-count.
18. Hold CALIBRATE switch up (+360.0/+180.0) and adjust (R79) for a display centered between +359.9 and +360.0.
19. Hold CALIBRATE switch up (+360.0/+180.0) and adjust (R20) for −3.600 V (±.3 mV) on the voltmeter.
20. Set RANGE selector to −180°/+180°.
21. Hold CALIBRATE switch down (000.0/−180.0) and adjust (R84) for a display of −180.0 plus or minus 1/2-count. Voltmeter should read −1.800 V ±2 mV.
22. Hold CALIBRATE switch up (+360.0/+180.0) and adjust (R22) for a display of +180.0 plus or minus 1/2-count. Voltmeter should read −1.800 V ±2 mV.
23. If readings are within ±2 mV, turn power off and reinstall display.
24. If steps 16 through 22 are out more than ±2 mV on the voltmeter, repeat steps 14 through 22 again. If voltmeter still indicates readings outside the specified limits, refer to the Corrective Maintenance instructions in paragraph 4.3.

4.2.5 Zero-Crossing Mid-Frequency Procedure

25. Turn power on, and set RANGE selector to −180°/+180°.
26. Connect a 1 kHz sine wave, 10 mV rms (28 mV p-p), into each input (Figure 4-1[A]. Program pins 23 & 24 to program ground.
27. Check 10:1 oscilloscope probe for dc zero, by connecting it to the circuit ground, and center trace on horizontal centerline of CRT. Set scope gain to 10 mV/cm, and sweep speed to 0.1 ms/cm.
28. Connect the scope probe to Channel A test point TP2 (Figure 4-3) of the Zero Crossing Board. The oscilloscope should display a waveform similar to the one shown in Figure 4-4[A].
29. Adjust DC BALANCE (R28) so that V_1 (Figure 4-4[A] is equal to V_2 (±10 mV)
30. Adjust CHOPPER BALANCE (R64) so that t_1 (Figure 4-4[A] is equal to t_2 (±1 μS).
31. Alternately perform steps 29 and 30 until the closest to optimum results are obtained.
32. Adjust TUNNEL DIODE (R63) until top of trigger is at zero volts dc (±1 mV) as shown in Figure 4-4[B].
33. Connect scope probe to test point TP5 adjust DC BALANCE (R119), CHOPPER BALANCE (R155), and TUNNEL DIODE (R154) and perform steps 29 through 32 for Channel B. Recheck oscilloscope for dc drift by connecting the scope probe to the phase meter ground and adjusting scope controls to reposition trace on horizontal center line.
34. If steps 25 through 33 have been followed correctly, the digital readout should indicate one half of plus and minus full scale (CALIBRATE switch up and down readings). This reading is called "out of case zero" in the rest of the manual.

Examples:

Calibrate "Up"	Calibrate "Down"	"Out of Case Zero"
+180.0	−180.0	000.0 (±.1°)
+180.2	−179.8	+000.2 (±.1°)
+180.2	−179.4	+000.4 (±.1°)

NOTICE

Do not be alarmed if the full scale values are not precise, the instrument is out of the case and will return to proper readings when case is replaced. It is important, however, that the "out of case zero" be displaced equally from the range extremes.

DO NOT READJUST
FULL SCALE VALUES AT THIS POINT

If "out of case zero" is not equally displaced repeat steps 25 through 33 and step 35 below. Go on to the Zero Crossing High Frequency Procedure; three or four tenths of a degree error could be caused by high frequency misalignment.

NOTICE

35. Increase the input signal amplitude to both channels to 1 V rms (2.8 V p-p). If reading changes more than ±0.1°, adjust PK-PK (R21) and (R112) for accurate time symmetry at test points 2 and 5, as shown in Figure 4-4[C].

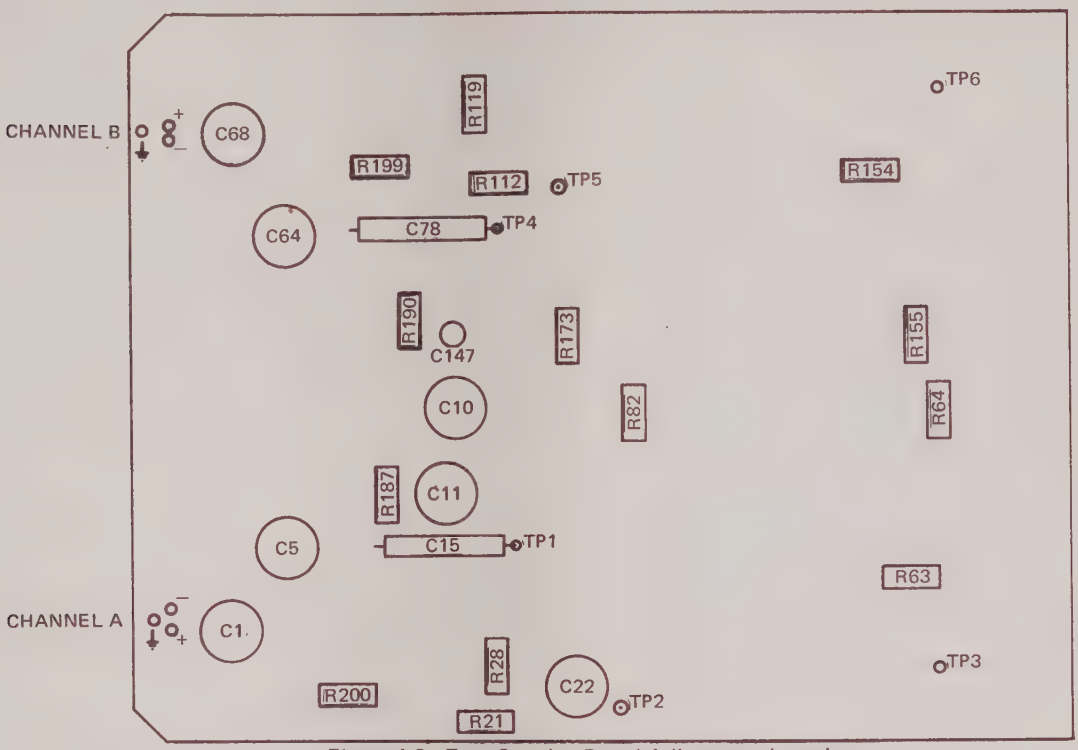


Figure 4-3. Zero Crossing Board Adjustment Locations

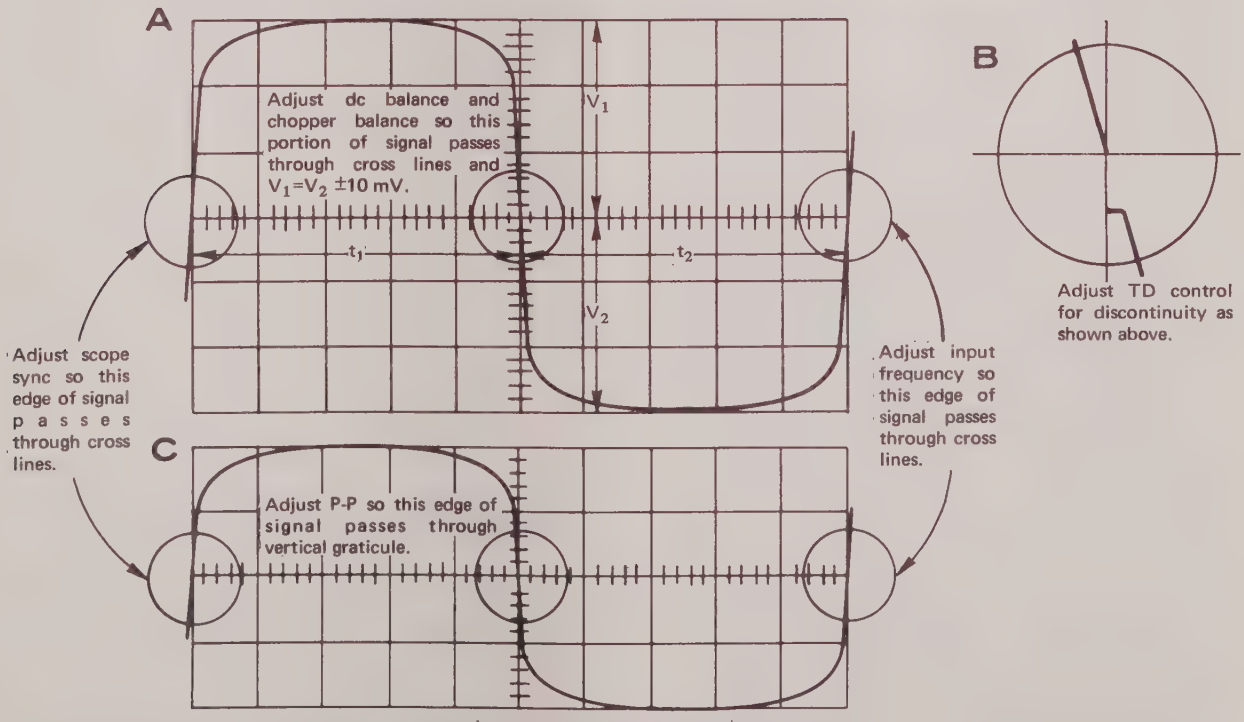

A
Adjust dc balance and chopper balance so this portion of signal passes through cross lines and $V_1=V_2$ ±10 mV.
V_1
V_2
t_1
t_2
Adjust scope sync so this edge of signal passes through cross lines.
Adjust input frequency so this edge of signal passes through cross lines.
B
Adjust TD control for discontinuity as shown above.
C
Adjust P-P so this edge of signal passes through vertical graticule.

Figure 4-4. Oscilloscope Calibration Displays

4.2.6 Zero-Crossing High-Frequency Procedure

36. Set RANGE selector to $-180^{\circ}/+180^{\circ}$ and remove all scope probes.
37. Apply a 10 mV rms sine wave, 80 kHz, into both channels, using the test configuration shown in Figure 4-1[A].
38. Adjust C22 until digital readout is equally displaced from range extremes for "out of case zero" (±0.2).
39. Increase input amplitude to 100 mV rms, increase input frequency to 800 kHz, and adjust C10 until the digital readout equals "out of case zero" ($\pm.4^{\circ}$).
40. Since steps 38 and 39 interact, they must be alternately performed until both readings, when going from one condition to the other, are within limits. Recheck steps 28 through 33 and, if necessary, readjust controls for proper indications.
41. Apply a 1 mV rms sine wave to both inputs, using the configuration shown in Figure 4-1[A] and, while watching the digital readout, vary the frequency from 1 kHz to 10 kHz. Record the reading at 1 kHz and the reading at 10 kHz. Determine the difference between the two readings, taking into account the polarities indicated, and record this as the "error span".

Examples:

1 kHz Readings	10 kHz Readings	Error Span
−000.2	+001.0	1.2°
+000.2	+001.1	$.9^{\circ}$
−000.2	−000.8	$.6^{\circ}$

42. Set input frequency back to 1 kHz at 1 mV rms and equally adjust Channel A TUNNEL DIODE (R63) and Channel B TUNNEL DIODE (R154) so that the digital display readout indicates one-third of the Error Span with a minus sign. (This would be -000.4° in the first example shown in step 41.)
43. Set input frequency to 10 kHz at 1 mV rms and display readout should indicate two-thirds of the Error Span with a plus sign. If the Error Span is not distributed one-third and two-thirds at 1 kHz and 10 kHz respectively, repeat steps 41 and 42.

4.2.6.1 ATTENUATOR FREQUENCY ADJUSTMENT

NOTE

Make sure the oscilloscope probes are properly compensated for lissajous operation. Check each probe with the scope calibrate signal, then connect both probes to the same signal and vary the frequency from 10 Hz to 1 MHz and make final adjustment for closed lissajous.

44. Set both VOLTS RMS ranges to .3-300 by applying an open or +.24 V to pins 23 and 24 of BCD connector and apply a 1 kHz 7 V rms sine wave to the positive input terminals as shown in Figure 4-1 [B]. Connect the probes of a dual channel scope, with lissajous capability, between the plus input terminal and test point TP1 of Channel A.
45. While varying the input frequency from 1 kHz to 10 kHz, adjust C1 for a closed lissajous.
46. Connect the scope probes to TP1 and TP4 of Channel B. Adjust C64 for a closed lissajous. The digital readout should now read within $\pm.2^{\circ}$ of reading obtained with 100 Hz input (switch to 100 Hz without changing amplitude and check). If it doesn't, repeat steps 45 and 46 until the readout is within this limit.

4.2.6.2 COMMON MODE REJECTION CALIBRATION

Channel B

47. Ground the amplitude range control (pins 23 and 24 BCD connector) placing the 755 in the .001-2 V rms range.
48. Apply a 10 kHz, 10 mV rms, sine wave to both inputs as shown in Figure 4-1 [C].
49. Connect scope probe to test point TP5 and circuit ground, and alternately adjust R190 and C147 for minimum signal. Increase input to 1 V rms and adjust for double input frequency at TP5.
50. Repeat steps 48 and 49 using a 100 kHz input. Adjusting only variable capacitor C147 for minimum signal at TP5.

Channel A

51. Ground the amplitude range control (pins 23 and 24 BCD connector) placing the 755 in the .001-2 V rms range.
52. Remove inputs from generator, both channel A and B. Connect both positive and negative inputs of channel A and B to circuit ground.
53. Connect scope to TP1 and adjust R187 for zero volts of offset with scope on 5 mV/cm range. Change phase range between $\pm180^{\circ}$ range and $0/360^{\circ}$ range. Adjust R187 for minimum dc variation between ranges, this may be slightly different from 0 volts.
54. Remove inputs from circuit ground. Connect generator to both channel A and B inputs as shown in Figure 4-1 [C]. Set generator for 10 kHz, 10 mV and adjust C11 for minimum signal at TP2. Increase input to 1 V rms and adjust C11 for minimum signal or frequency doubling.
55. Repeat step 54 using a 100 kHz input adjusting only variable capacitor C11 for minimum signal.

4.2.6.3 ATTENUATOR COMMON MODE REJECTION ADJUSTMENT

56. Set both VOLTS RMS ranges to .3-300 by applying an open or +2.4 V to pins 23 and 24 of BCD con- and apply a 7 V rms 250 Hz sine wave to both inputs as shown in Figure 4-1[C].
57. Connect scope probe to test point TP2, and circuit ground and adjust R200 for minimum signal.
58. Increase input frequency to 25 kHz, and adjust C5 for minimum amplitude at TP2.
59. Connect scope probe to test point TP5, decrease input frequency to 250 Hz, and adjust R199 for minimum signal.
60. Increase input frequency to 25 kHz, and adjust C68 for minimum amplitude at TP5.
61. Repeat steps 51 through 55 if needed.

Auto Ranged Calibration

With the volt meter connected between the wiper of R16 and ground, adjust R16 for 3.5 volts ±1%. Connect the volt meter between the wiper of R12 and ground and adjust R12 for 0.1 volts ±10 mV.

4.2.7 Phase Lock Calibration Procedure

After calibration of the zero crossing board, logic and power supply board, and auto ranging board and after verification of phase measurement performance, the phase lock board can be calibrated with the following procedure:

62. Interconnect the 755 with a reference generator Wavetek Model 157 or equal and a slaved Model 157 (with phase lock capability) as shown in Figure A-1. Set both function generators at 400 Hz ±.1% and amplitude at 1 V rms.
63. Select 755 switches and program connectors as follows:

    Rear Panel—
    (a) Continuous Read
    (b) Range Select
    (c) —180/+180 or Ext. Program

    Front Panel —Phase Lock

    BCD Connector (J2) pin (32) — (Loop time constant) to program ground pin (25). All other pins +2.4 V to +5 V or open.

    Phase program connector (J8)—All control pins open.
64. After ½ hour warm-up, remove bottom cover of 755 and perform following steps.
65. Place R21 and R54 in center position.
66. Check calibrate 000.0° and 360.0° and +180.0° and —180.0° for proper adjustment.
67. Check for phase locking of two input waveforms by placing both inputs to an oscilloscope in the chop mode and noting that both waveforms are stationary.

NOTE

If not phase locked, check interconnections for proper channel input to 755, (Reference to Channel B, controlled frequency to Channel A.) and phase lock connector to 157, and that system is in phase locked mode.

68. Adjust R3 for 000.0° degrees phase lock.
69. Place voltmeter between junction of R5 and R6 and gnd. With system in 0-360° range and calibrate switch to +360.0°. Adjust R6 for —0.16 volts.
70. Place 755 in 0-360° range and program 180° phase shift by grounding (J2) pin (31).
71. Adjust R50 for 180.0° on digital readout.
72. Place 755 in ±180° range.
73. Program +90° by grounding J2 pin 29 and adjust R48 for 90.0°.
74. Program +30° by grounding J2 pin 28 and adjust R46 for 30.0°.
75. Program —90° by grounding J2 pin 27 and adjust R44 for 90.0°.
76. Program —30° by grounding J2 pin 26 and adjust R42 for 30.0°.
77. Place instrument in the ±180° range and program into the Continuous Phase Shift pin (33) a dc voltage equivalent to 90.0° (9.00 V) and adjust R39 for 90.0°.
78. The 755 phase meter with phase lock option has a capture range of ±2% frequency difference for 0° phase program.

NOTE

The capture range is defined for zero degrees phase shift, however these adjustments insure optimal capture frequency with all phase shifts. The amplitude of the reference signal may vary between 1% and 100% of full scale without effecting capture frequency and the amplitude of the slave frequency may vary between 10% and 100% of full scale.

To adjust for maximum capture range complete the following procedure.

79. Place 755 in ±180° range with no phase shift programmed (0.0 degrees).
80. Adjust R54 to its maximum clockwise position.
81. Adjust R21 to its maximum counterclockwise position.

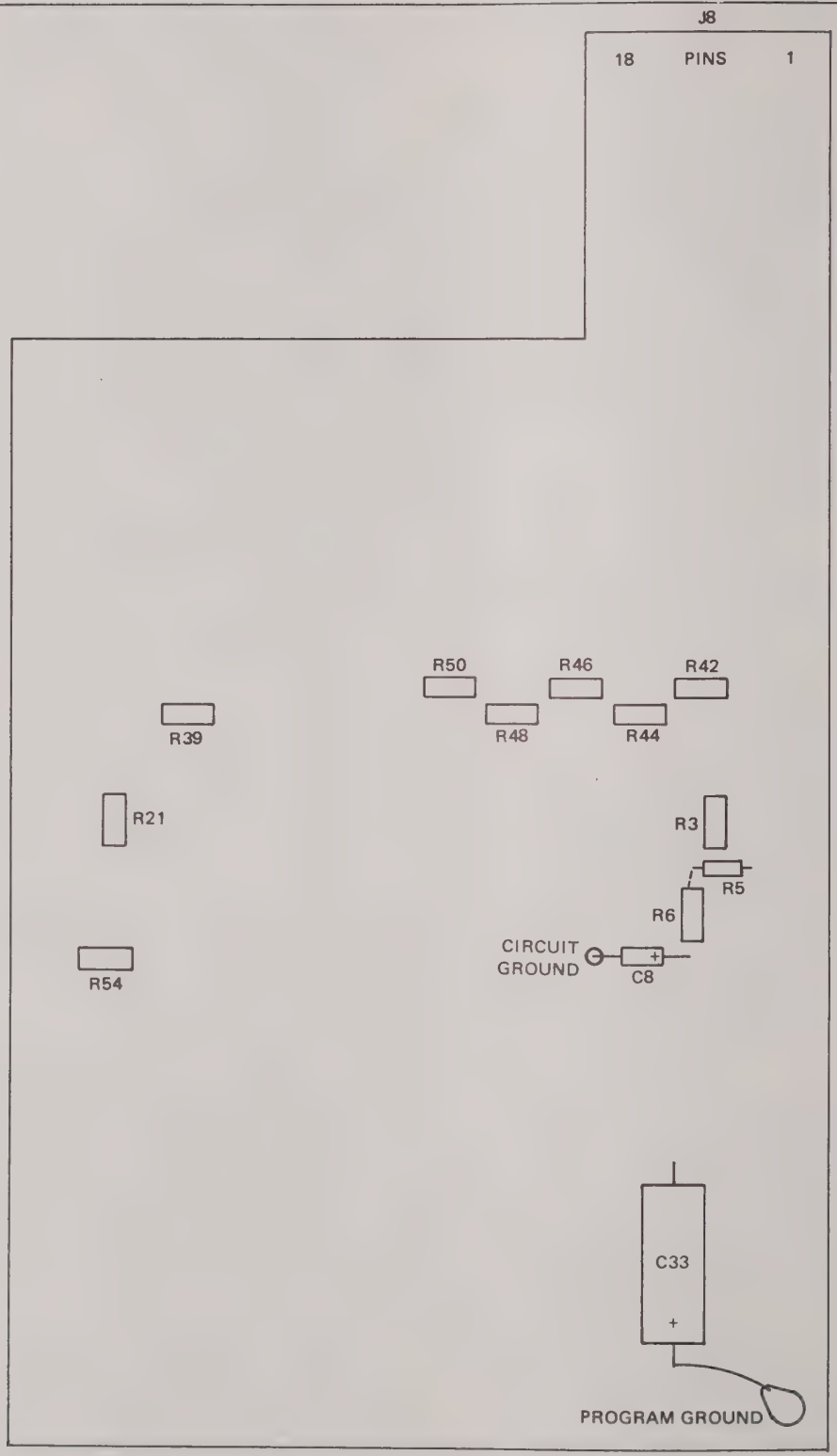


Figure 4-5. Calibration Locations on Phase Lock Board

82. Set reference frequency to 408 Hz and slaved frequency to 400 Hz.
83. Program +30° by grounding J2 pin 28 on BCD connector.
84. Alternately depress the front panel phase lock and open loop pushbuttons until the phase does not read +30 ±.5° on readout in the phase lock mode. If 755 never fails to lock, leave R21 in ccw position and continue on to 82.
85. Adjust R21 clockwise until this reading equals +30 ±.5°.
86. Set reference frequency to 400 Hz and the slaved frequency to 408 Hz and program −30° by grounding J2 pin 26 on BCD connector.
87. Alternately depress the phase lock and open loop pushbuttons until the phase does not read −30±.5°. If the phase meter always locks to −30 ±.5° do not move R54. If it locks on a different phase, adjust R54 counterclockwise until phase reads −30 ±.5°. If 755 never fails to lock leave R21 in clockwise position and continue on to 82.

4.3 CORRECTIVE MAINTENANCE

If the Model 755 Phase Meter appears to be operating abnormally, and an investigation of input/output connections, as well as a calibration check, do not cure the problem; follow the trouble-shooting procedure outlined below.

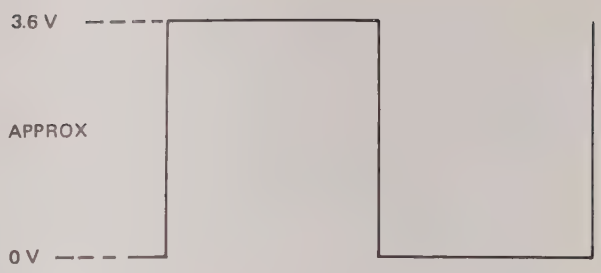
Trouble	Check
1. Readout jumping around when no input signal is applied.	Normal operation, the high sensitivity of the input picks up external 60 Hz noise.
2. Readout scattering occasionally with low input amplitude and/or frequency.	Noise spikes are riding on input signal or signal-to-noise ratio is too high. Put 0.1 μF capacitors, or matched filters, across inputs.
3. Readout scattering randomly with input signal applied.	a. Check that phase angle is not within 2° of RANGE extreme. Use other RANGE setting. b. Reduce ground loops, and use differential inputs isolating grounds.
4. Erroneous phase reading.	a. Check both VOLTS RMS settings. Overdrive causes phase errors. b. Quick check CALIBRATE limits. c. If "a" and "b" do not help, apply same input to both channels, select −180°/+180° RANGE and, if reading is not 000.0, recalibrate Zero Crossing Board.
5. Display not lighted when POWER is set to ON.	Check fuse. Check +180 V, ±15 V, ±3.6 V, and +5 V power supplies.
6. Two digits light in same lamp.	Defective display lamp.
7. Display locked on maximum or minimum full scale regardless of inputs.	a. If locked on maximum, Channel A Zero Crossing has no output. b. If locked on minimum, Channel B Zero Crossing has no output. c. If not "a" or "b" check IC4 on the Logic and Power Supply Board.
8. Input loading circuit being measured due to low input impedance.	Input FET Q1, Q2, Q14, or Q15 has been damaged. Replace with MPF104 or 2N5458 or equivalent.
9. System does not phase lock.	a. Check proper phase lock connector. b. When the 755 is operating in phase locked mode with external programming, obtain phase lock by programming 000.0° phase shift. System should not be in auto range when in phase lock mode.

If the instrument is not operating properly, and the above steps do not solve the problem, recalibrate the instrument as described in paragraph 4.2. If recalibration does not solve the problem, follow the procedure outlined below.

1. First check all power supplies for proper operation. If any are malfunctioning, refer to the Circuit Description as well as the schematic when trouble shooting the supply.
2. With 1 kHz 1 V rms sine wave applied to both inputs, look at Zero Crossing test points TP3 and TP6. If 1 V

pulses at 1 kHz are not observed, read Circuit Description and refer to the schematic for trouble shooting.

3. If the proper pulses are seen in step 2 above, look at the junction of R65, R66, and R68. This point should show a waveform like that pictured.
4. If the dc OUTPUT −10 mV/DEG is correct but the digital display is incorrect, recheck +180 V, +5 V, and ±3.6 V supplies. Refer to the timing diagram (Figure 3-6) and Circuit Description given in paragraph 3.2.3.



INPUT 0 V rms, 1 kHz, 0°
RANGE set to −180°/+180°

SECTION 5
DIAGRAMS ADDENDUMS AND PARTS LIST

5.1 DIAGRAMS

The schematic diagrams within this manual are, wherever possible, arranged in the sequence followed in the circuit description. Whenever assembly drawings are included, they are positioned adjacent to the schematics for maximum information presentation and minimum page flipping. Additional voltage or waveform information, beyond that given in the circuit description, may be shown on the schematic diagrams, at test points and key locations throughout the instrument.

5.2 ADDENDUMS

Under WAVETEK's product improvement program, the latest electronic designs and circuits are incorporated into each WAVETEK instrument as quickly as development and testing permit. Because of the time needed to compose and print instruction manuals, it is not always possible to include the most recent changes in the initial printing. Whenever this occurs, addendum pages are prepared to summarize the changes made under a WAVETEK Engineering Change Notice (ECN) and these ECN pages are inserted immediately inside the rear cover. If no such pages exist, the manual should be correct as printed.

5.3 PARTS LISTS

Whenever possible, an assembly drawing and the associated parts list are kept to one piece of paper or are positioned for maximum information presentation. The following list of manufacturers should be used in conjunction with the parts lists. The abbreviations shown below are used in the "Manufacturer Key" column on the parts lists.

DRAWINGS

The following assembly drawings (with parts lists) and schematics will be included at the rear of this manual, in the arrangement shown below:

LEFT PAGE

CHASSIS ASSEMBLY
352-000 Sheet 1 of 2

LOGIC AND POWER SUPPLY ASSEMBLY
352-010

ZERO CROSSING BOARD ASSEMBLY
352-011

DIGITAL BOARD ASSEMBLY
352-012

PHASE LOCK BOARD ASSEMBLY
352-014 Sheet 1 of 2

PHASE LOCK BOARD SCHEMATIC
352-214

AUTO RANGE BOARD ASSEMBLY
352-015

ISOLATION BOARD ASSEMBLY
352-016

INPUT PROTECTION BOARD ASSEMBLY
352-017

ANALOG BOARD ASSEMBLY
270-011C

RIGHT PAGE

CHASSIS SCHEMATIC
352-200

LOGIC AND POWER SUPPLY SCHEMATIC
352-210

ZERO CROSSING BOARD SCHEMATIC
352-211

DIGITAL BOARD SCHÉMATIC
352-212

PHASE LOCK BOARD ASSEMBLY
352-014 Sheet 2 of 2

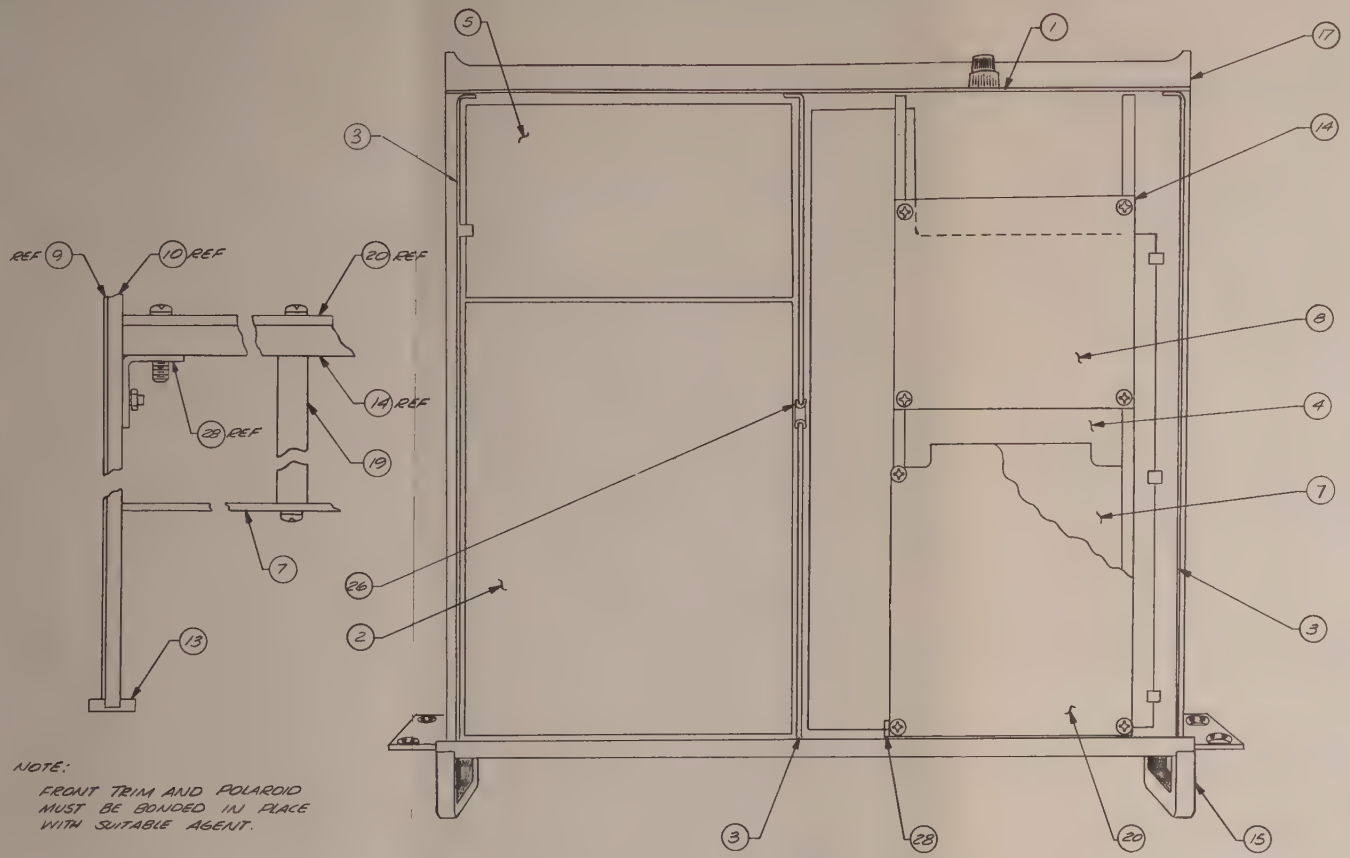
REAR PANEL ASSEMBLY
352-000 Sheet 2 of 2

AUTO RANGE BOARD SCHEMATIC
352-215

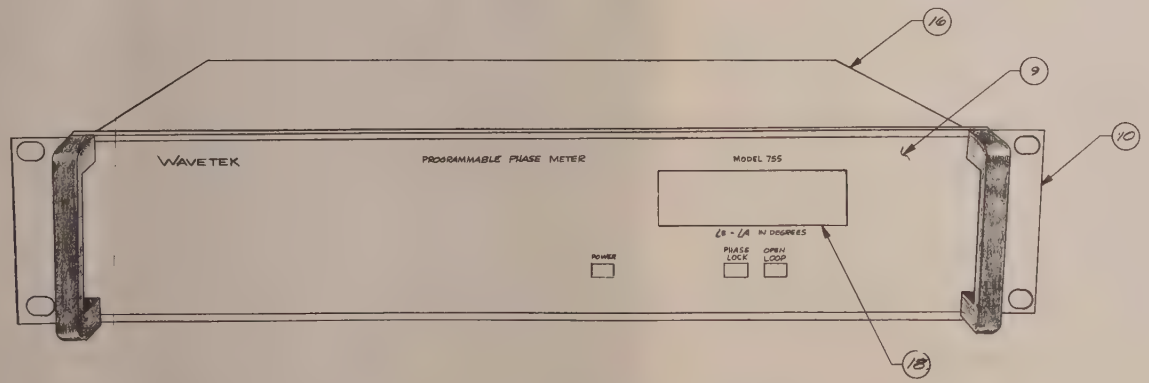
ISOLATION BOARD SCHEMATIC
352-216

INPUT PROTECTION BOARD SCHEMATIC
352-217

ANALOG BOARD SCHEMATIC
270-211B



NOTE:
FRONT TRIM AND POLAROID MUST BE BONDED IN PLACE WITH SUITABLE AGENT.



NOTE
1. ASTERISK(*) INDICATES ITEM NOT SHOWN

PARTS LIST

ITEM	REF DES	DESCRIPTION	MFGR	MFGR NO.	QTY
1		REAR PANEL ASSY	WAVETEK	D352-000	1
2		POWER SUPPLY BD		D352-010	1
3		SIDE & CENTER PLATE		C755-001	3
4		PHASE LOCK BD		D352-014	1
5		AUTO RANGE BD		D -015	1
6		ZERO CROSSING BD		D -011	1
7		DIGITAL BOARD		D -012	1
8		ISOLATION BOARD		D -016	1
9		FRONT PANEL		C -301	1
10		SUB PANEL		C -302	1
11					
12					
13		FRONT TRIM		B755-307	2
14		READOUT BAR		B -316	2
15		HANDLES		B -317	2
16		TOP COVER		C -318A	1
17		BOTTOM COVER		C -322A	1
18		READOUT WINDOW		A -323	1
19		NIXIE STANDOFF		A750-313	4
20		ANALOG BOARD		D270-011	1
21					
22					
23					
24					
25					
26		GROMMET	PLASTRON	MS-21266-1	A/R
27					
28		BRACKET	ZIERICK	260	2
29					
30					

	C	1165	B.F.	12-22-71
	rev.	ecn	by	date app

tolerance unless otherwise specified: XXX ± .010, XX ± .030
scale N/A
material
finish

WAVETEK San Diego, Calif.
by GRAY date 2-9-71 app
title: CHASSIS ASSY
model no. 755-S-200
dwg no. SHT 1 OF 2 D352-000
rev C

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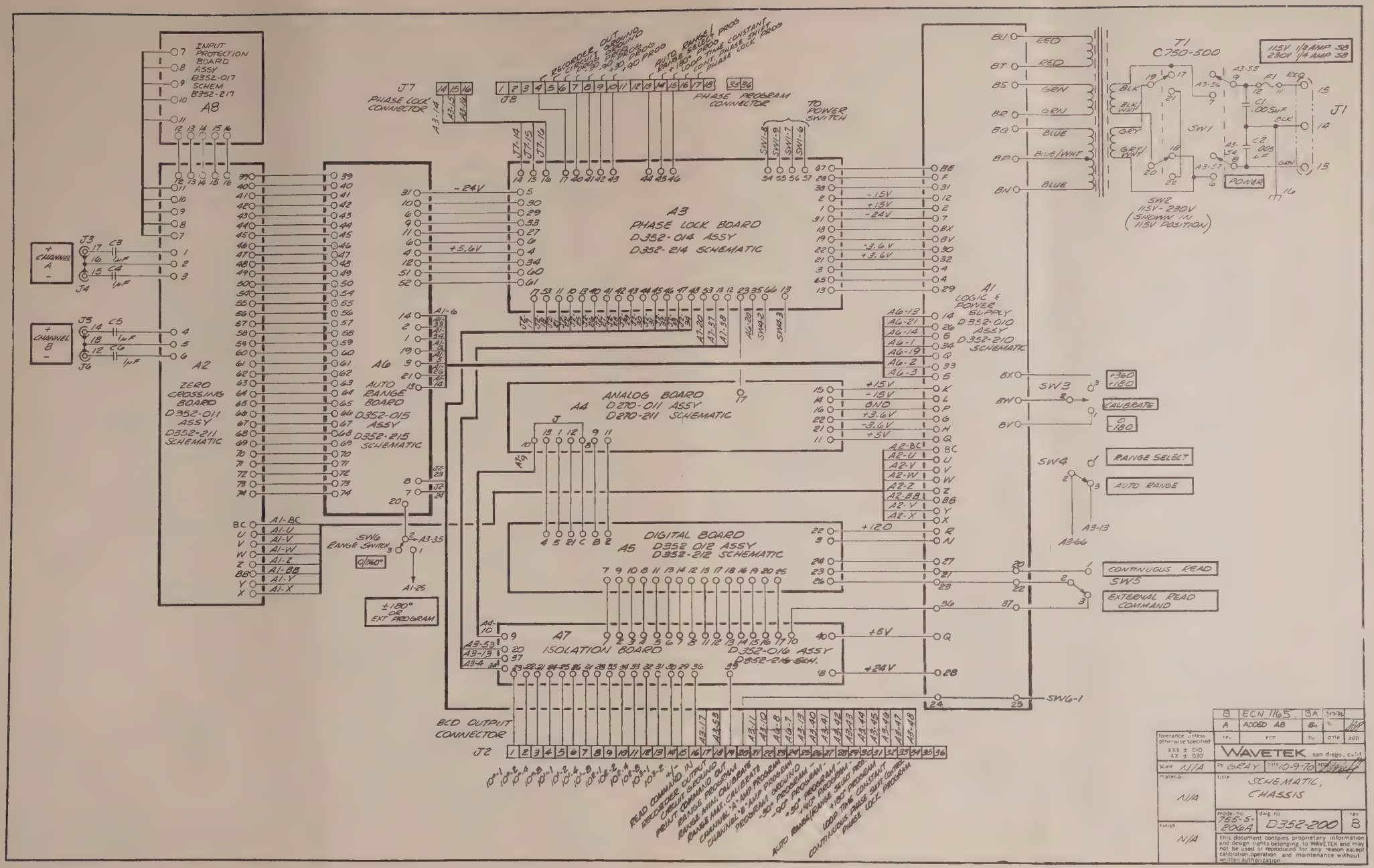

B	ECN 1165	BA	7-17-72		
A	ADDED A8	BA	7-1-72		
rev	ecn	by	date	app	

tolerance unless otherwise specified: XXX ± .010, XX ± .030

WAVETEK san diego, calif

scale N/A | by GRAY | date 10-9-70 | approved

material: N/A

title: SCHEMATIC, CHASSIS

model no 755-S-206A | dwg no D352-200 | rev B

finish: N/A

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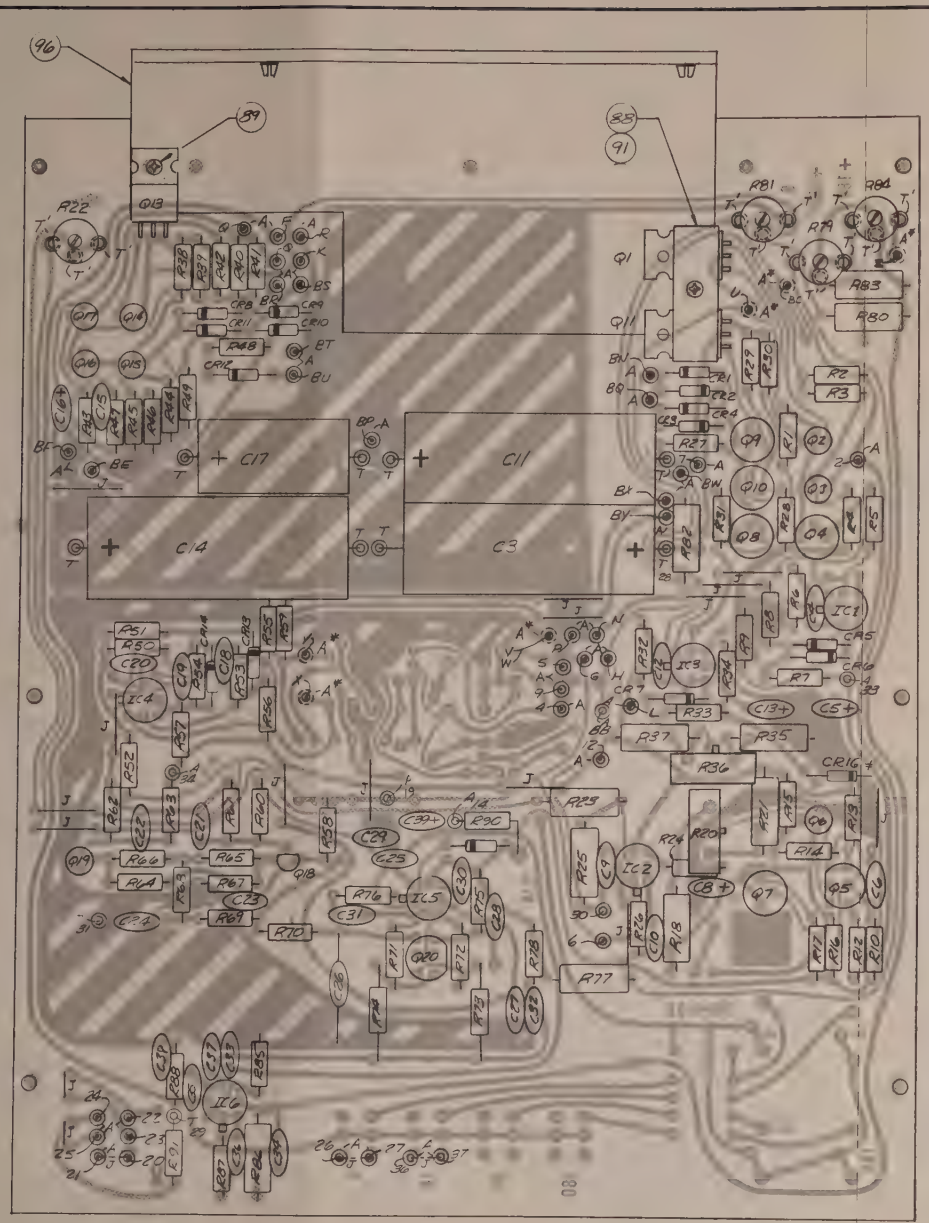

PARTS LIST

ITEM	REF DES	DESCRIPTION	MFGR	MFGR NO	QTY
1		CAPACITORS			
2	C9, C30, C35	CERAMIC DISC, 1000V, 10% 220PF	CRL	DD221	3
3	C8, C22	22PF		DD220	4
4	C6 C20 C23	30V 1% .1µF		UK20-104	3
5	C4, C10, C12, C24, C28, C31, C32, C34, C38, C39	50V 10% .005µF		CK-502	10
6	C25	1000V, 10%, 560pF		DD561	1
7	C17	ELECTROLYTIC 350V 4µF	SPRAGUE	TVA-1601	1
8	C5, C19	35V 27µF		19D276X0035G8	2
9	C8, C14, C29	15V 22µF		196D226X0015FB	3
10	C3 C11	35V 1000µF		39D108G035GH	2
11	C16	15V 4000µF		39D408G015JL	1
12	C33 C36 C38 C37	CERAMIC DISC 50V 10% .01µF	CRL	CK103	4
13	C24	1KV, 10%, .005µF			1
14	C26	100pF		DD101	1
15					
16	CR1-CR4, CR8-CR11	DIODES	SEMTECH	SCE-1	8
17	CR5-CR7, CR12		FAIRCHILD	FD6666	4
18	CR12		SEMTECH	SCE-2	1
19	CR13, CR14		HP	HP 2811	2
20	CR16	DIODE, ZENER (-39)	DIXON	IN4581	1
21					
22					
23		INTEGRATED CIRCUITS			
24	IC1-IC3 IC4, IC6	µA709	FAIRCHILD	µA709	5
25	IC4	CµL914		CµL914	1
26					
27					
28	Q1 Q13	TRANSISTOR TIP29	TI	TIP-29	2
29	Q11	TIP30		TIP-30	1
30	Q2, Q3, Q6 Q14, Q19	2N3565	FAIRCHILD	21N3565	7
31	Q4, Q5 - Q10	2N3638		2N3638	4
32					
33	Q18	2N3640		2N3640	1
34	Q7	2N3642		2N3642	1
35	Q12	2N3646		21N3640	1
36	Q5 Q20	TD101	SPRAGUE	TD101	2
37					
38					
39	R20	POTENTIOMETER 100Ω	CRL	BA1603-801	1
40	R36	1K		BA1603-803	1
41	RT2, RT3 RB1	TYPE S - 500Ω (-41)	A/B	SV-5011	3
42	RB4	1K (-45)		SV 1021	1
43					
44					
45		WIRE WOUND PRE-AGED			
46	R18	1%, 237K	MICRO OHM	TYPE 143	1
47	R35	7.70K			1
48	R37	9.53K			1
49	R23	9.75K			1
50	R21, R25, R27, REC, R36	10K			5
51	DRT, R83	19.6K			2
52					
53					
54		RESISTORS			
55	R40, R41	CARBON, 1/2W, 5%, 3.9Ω	STACKPOLE	RC20GF3R9J	2
56	R2, R30, R58	6.8Ω		GRBJ	5
57	R73, R74	10%, 2M		205K	2
58					
59					
60					
61	R52	METAL FILM, 1/8W, 1%, 33.2Ω	CORNING	RN55D	1
62	R46, R78, R88, R90	100Ω			4
63	R91	249Ω			1
64	R17, R42, R50, R51	332Ω			4
65	R3, R29	464Ω			2
66	R43	681Ω			1

PARTS LIST

ITEM	REF DES	DESCRIPTION	MFGR	MFGR NO	QTY
67					
68	R45, R61 R62, R71, R72	METAL FILM, 1/8W, 1%, 1.00K	[illegible]	[illegible]	[illegible]
69	R48	1/4W 1.21Ω			
70	R6, R26, R42, R55, R59, R76 R87	1/8W 1%			
71	R12, R33 R34	3.3K			
72	R47	4.75K			
73	R16	5.11K			
74	E23 R85	9.53K			
75	R1, R4, R5, R7, R28 R2, R36, R39, R40, R50 R44-R49, R44-R67	1.00K			
76	R14	1.18K			
77	R13, R31 R32	1.69K			
78	R17, R8 R34	2.21K			
79	C22, R17	5.62K			
80	R15	6.34K			
81	R56, R57	7.15K			
82	R68-R70	8.66K			
83	R75	11.5K			
84	R49	1MA			
85					
86					
87		TERMINAL INSULATOR		MS 19...	
88			WISE SCREW	[illegible]	
89		NYLON SCREW	SMITH	2505	1
90		TRANSISTOR INSULATOR	WAVETEK	A740-307	2
91		HEATSINK	WAVETEK	A130-311	2
92		TRANSIPADS	WILCOX ROSS	10128W	6
93	A, A*	AMP PINS	AMP	61182-2	1
94	T	TERMINALS	USECO	20108-1	12
95	T'	TERMINALS	USECO	20058-1	12
96		HEATSINK	WAVETEK	9755-320A	1
97		PRINTED CIRCUIT BOARD	WAVETEK	740-110C	1

NOTES UNLESS OTHERWISE SPECIFIED

1. A* INDICATE AMP PINS INSTALLED ON CIRCUIT SIDE
2. LETTERED AND NUMBERED DESIGNATIONS ARE FOR INTERWIRING PURPOSES SEE SCHEM 755-200

rev	ecn	by	date	app.
A	ECN 156	[illegible]	[illegible]	

tolerance unless otherwise specified .XXX ± .010 XX ± .030

scale N/A

material N/A

finish N/A

WAVETEK san diego calif

by SCHEV date 6-...70 app. [illegible]

title ASSEMBLY LOGIC + POWER SUPPLY BD

model no. 755-S 806 | dwg no. C3E2-010 | rev A

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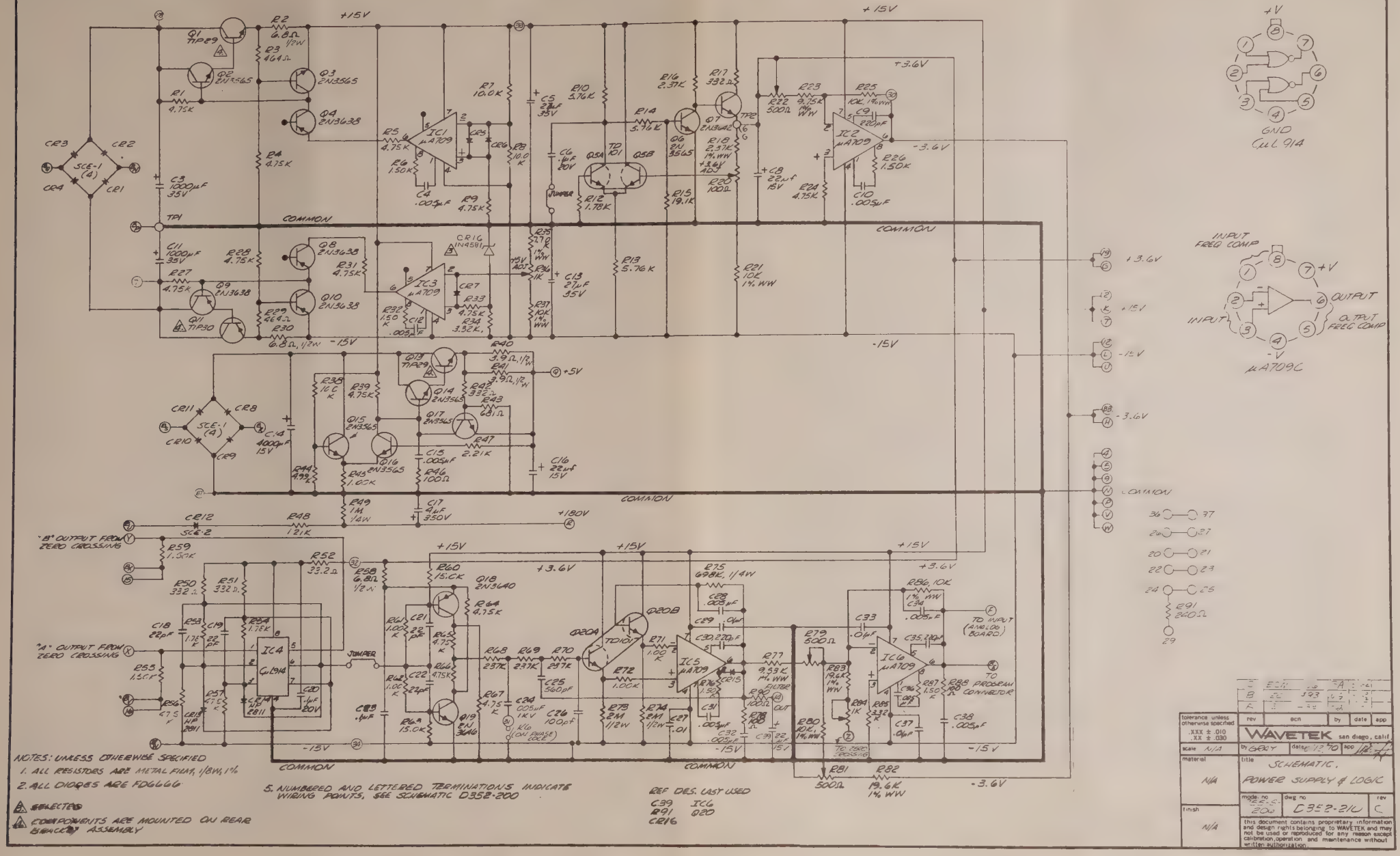
+15V
-15V
+3.6V
-3.6V
+180V
+5V
COMMON
TP1
SCE-1 (A)
SCE-2
IC1 µA709
IC2 µA709
IC3 µA709
IC4 CL914
IC5 µA709
IC6 µA709
Q1 TIP29
Q2 2N3565
Q3 2N3565
Q4 2N3638
Q5A TD101
Q5B TD101
Q6 2N3565
Q7 TIP29
Q8 2N3638
Q9 2N3638
Q10 2N3638
Q11 TIP30
Q13 TIP29
Q14 2N3565
Q15 2N3565
Q16 2N3565
Q17 2N3565
Q18 2N3640
Q19 2N3640
Q20A TD101
Q20B TD101
CR16 (IN4581)
JUMPER
"A" OUTPUT FROM ZERO CROSSING
"B" OUTPUT FROM ZERO CROSSING
TO INPUT (ANALOG BOARD)
TO PROGRAM CONNECTOR
TO ZERO CROSSING
INPUT FREQ COMP
OUTPUT
OUTPUT FREQ COMP
GND (µL 914)
µA709C
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE METAL FILM, 1/8W, 1%
2. ALL DIODES ARE FDG666
3. SELECTED
4. COMPONENTS ARE MOUNTED ON REAR BEHIND ASSEMBLY
5. NUMBERED AND LETTERED TERMINATIONS INDICATE WIRING POINTS, SEE SCHEMATIC D352-200
REF DES. LAST USED
C39 IC6
R91 Q20
CR16
tolerance unless otherwise specified .XXX ± .010 .XX ± .030
WAVETEK san diego, calif
scale N/A
by GBOY date 12 '70 app
material N/A
title SCHEMATIC, POWER SUPPLY & LOGIC
mode no 352-S-200
dwg no D352-21L
rev C
finish N/A
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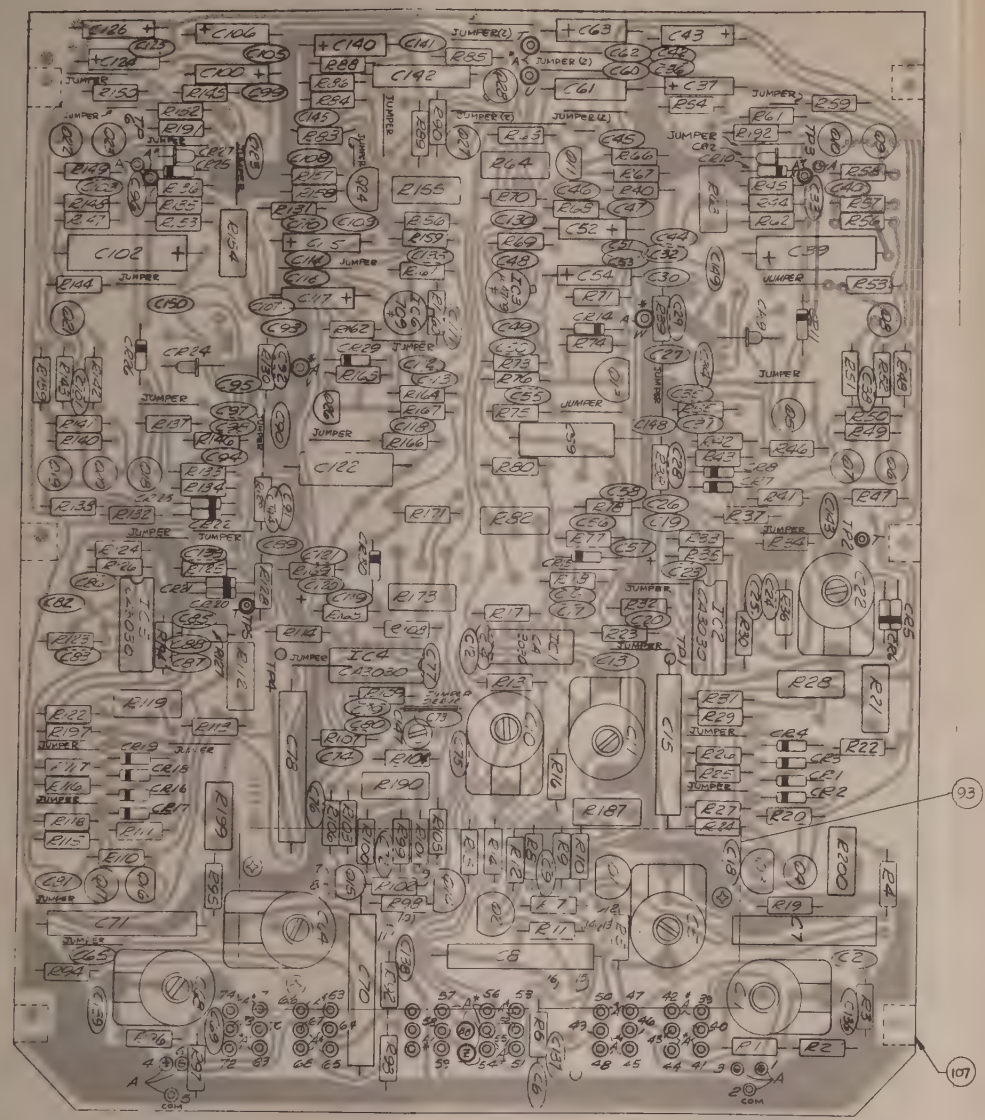

NOTES: UNLESS OTHERWISE SPECIFIED

1. "A" INDICATES AMP PIN MOUNTED ON CIRCUIT SIDE, "A" AMP PIN MOUNTED FROM NEAR SIDE.
2. FOR INTERCONNECTIONS REFER TO SCHEMATIC D352-200
3. LETTER DESIGNATIONS ARE INTERCONNECTION POINTS.

PARTS LIST

NO	REF DES	DESCRIPTION		MFGR	MFGR NO	QTY
1	C2, C6 C63 C64, C73 C85	CERAMIC DISC 1000V	5 PF	CRL	DD-050	6
2	C130, C135		1.5 PF	SPRAGUE	10TCC-V1S	2
3	C23–C25, C76 C80–C82		10PF	CRL	DD-100	7
4	C18, C81		15PF		DD 150	2
5	C14, C17 C61 C77 C82, C143, C152 C112, C139, C149		22PF		DD 220	7
6	C16, C38, C47 C79, C101, C110		100PF		DD-.01	6
7	C48, C111		220PF		DD-221	2
8	C33 C34 C96, C97		330PF		DD-331	4
9	C40, C36 C103, C119		470PF		DD471	4
10						
11	C35, C115 C136, C146	CERAMIC DISC 1000V	1500PF	CRL	DD-152	6
12	C28 C30 C91 C98		.05µF		CK-503	4
13	C5, C31, C36 C42, C57, C82 C58, C60, C95 C62, C75, C104 C114, C116, C125 C129, C141 C143, C98, C99		50V .01µF		CK-103	20
14	C12, C13, C19 C20 C31, C44 C45, C59 C69, C75, C76 C82, C83 C94 C107 C108 C113 C121		20V .1µF		UK20-104	18
15	C37, C43, C52 C54, C61 C63, C100 C106, C115, C117 C124, C126 C140	ELECTROLYTIC 15V	5µF	SPRAGUE	S000501G016BA1	13
16	C57, C120	TANTALUM	33µF		196D336X0015 FB	2
17	C89, C102	ELECTROLYTIC 16V	100µF		S000107G016DC1	2
18	C58, C122	MYLAR 100V 10%	.1µF	CDE	WMF-1P1E	2
19	C7, C8, C15 C70, C71, C78	MYLAR 200V 1%	1µF	CDE ELECTRO CABLE	210BIC-105F	6
20	C22, C101	VARIABLE CAPACITOR	4.5-25PF	ERIE	503-001-37A	3
21	C46, 144	SELECTED VALUE				2
22	C147	VARIABLE CAPACITOR	3.5-15 PF	STETTNER	75-TRIKO-02	1
23	C26, C27, C33 C83, C90, C121	CERAMIC DISC 50V	.1µF	CRL	CK-104	6
24	C46, C109	MYLAR 50V	.1µF	GE	69F13AA104	2
25	C142	MYLAR 100V	.0474µF	C DE	WMF 1547	1
26	C1, C5, C49, C68	VARIBLE CAPACITOR	3-12	ERIE	503-001-17A	4
27	CR1-CR8, CR7, CR8, CR10, CR14-CR19, CR22, CR23 & CR25, CR26, CR29, CR30	DIODE		FAIRCHILD	FD6666	18
28	CR11, CR26				1N34A	2
29	CR12, CR27			G.E.	IN3716	2
30	CR9, CR24	TUNNEL			IN3717	2
31	CR5-6 CR20-21		(-42)	H.P.	HP2811	4
32						
33						
34						
35						
36	IC3, IC6	INTEGRATED CIRCUIT	-75	FAIRCHILD	UA709	2
37	IC1 IC4		(-40)	RCA	CA3030	2
38	IC2 IC5		(-40)		CA3080	2
39						
40						
41						
42						
43	Q5 Q10, Q16 Q23	TRANSISTORS		FAIRCHILD	2N3640	4
44	Q4, Q6-Q9 Q17, Q19-Q22 Q27				2N3646	11
45	Q28			MOTOROLA	2N4851	1
46	Q11, Q18 Q24, Q26				MPF-104	4
47	Q1, Q2 Q14 Q15		(-37)		MPF-104	4
48	Q3 Q16		(-38)		MPF-104	2
49						
50						
51						
52	R63 R154	POTENTIOMETER	500Ω	CRL	BA1203-802	2
53	R199 R200		1K		-803	2
54	R21 R112 R190 R187		10K		-805	4
55	R28 R72 R114 R173		100K		-819	4
56	E64, R135		10K	A/B	FR103M	2
57						

PARTS LIST

NO	REF DES	DESCRIPTION	MFGR	MFGR NO	QTY
58	R48, R50 R66 R77, R78 R98, R139 R145, R146, R160, R162	METAL FILM, 1/8W, 1%, 10Ω	CORNING	RN550	11
59	R89			68.1Ω	1
60	R3, R6, R19, R32, R58, R64, R97, R107, R110, R123, R189			100Ω	10
61	R27, R132			150Ω	4
62	R85			221Ω	1
63	R47, R55, R57, R138, R146, R148			464Ω	6
64	R45, R47, R67, R68, R78, R83, R84, R132, R158, R159, R160			1.00K	11
65	R17, R18, R35, R36, R59, R69, R108, R109, R111, R112, R150, R160			1.50K	12
66	R53, R90, R148			2.21K	3
67	R8, R99			2.87K	2
68	R62, R65, R103, R154, R191, R192			3.32K	6
69	R34, R125			3.92K	2
70	R22, R30, R90, R92, R52, R113, R135, R140, R179-R183			4.75K	10
71	R42, R43, R133, R134			4.99K	4
72	R25, R116			5.76K	2
73	R10, R12 R101, R103			6.81K	4
74	R9, R100			7.50K	2
75	1284			9.09K	1
76	R4, R95			9.53K	2
77	R2, R20, R26 R29, R57, R96, R117, R80 R93, R111, R113, R142, R147, R168, R171			10.0K	16
78	R14, R15, R105, R106			(-9) 10.0K	4
79	R73, R77 R104, R107			(-39) 12.1K	4
80	R86			19.1K	1
81	R24, R115			21.5K	2
82	R40, R46, R131, R137			27.4K	4
83	R31, R33, R75, R77 R124, R166			47.5K	6
84	R50, R141			63.4K	2
85	R76, R167			150K	2
86	R74, R165			221K	2
87	R23, R114		1/4W, 464K	RN60D	2
88	R7, R11 R37-R39, R98, R162, R128-R130		11MΩ		10
89	R70, R161	CARBON, 1/2W, 10%, 2.2M	STACKPOLE	RC20GF225K	2
90	R1 R5, R32, R96	METAL FILM 1/4W 1% 1M	CORNING	RN60D	4
91					
92					
93		INPUT PROTECTION ASS'Y	WAVETEK	352-017	1
94		CIRCUIT BOARD	WAVETEK	740-11E	1
95					
96	⊙	TERMINALS	USECO	20108-1	2
97					
98	⊙ A	AMP PINS	AMP	61182-2	52
99					
100					
101		CHASSIS FASTENER	USECO	15918-1	6

E	1167	BA	2-17-71
E	1099	BA	2-17-71
D	ECN 580	JH	9/15/70
C	ECN 493	JH	8/2/70
B	457	JH	9/14/70
A	REVISED AMP NOS ADDED INPUT PROTECTION ASSY	BA	8/24/70

Tolerance unless otherwise specified: XXX ± .010, XX ± .030

WAVETEK

Date 11-22-68 Drawn [illegible]

Material —

Finish N/A

755-S-200A

Dwg # D352-011 F

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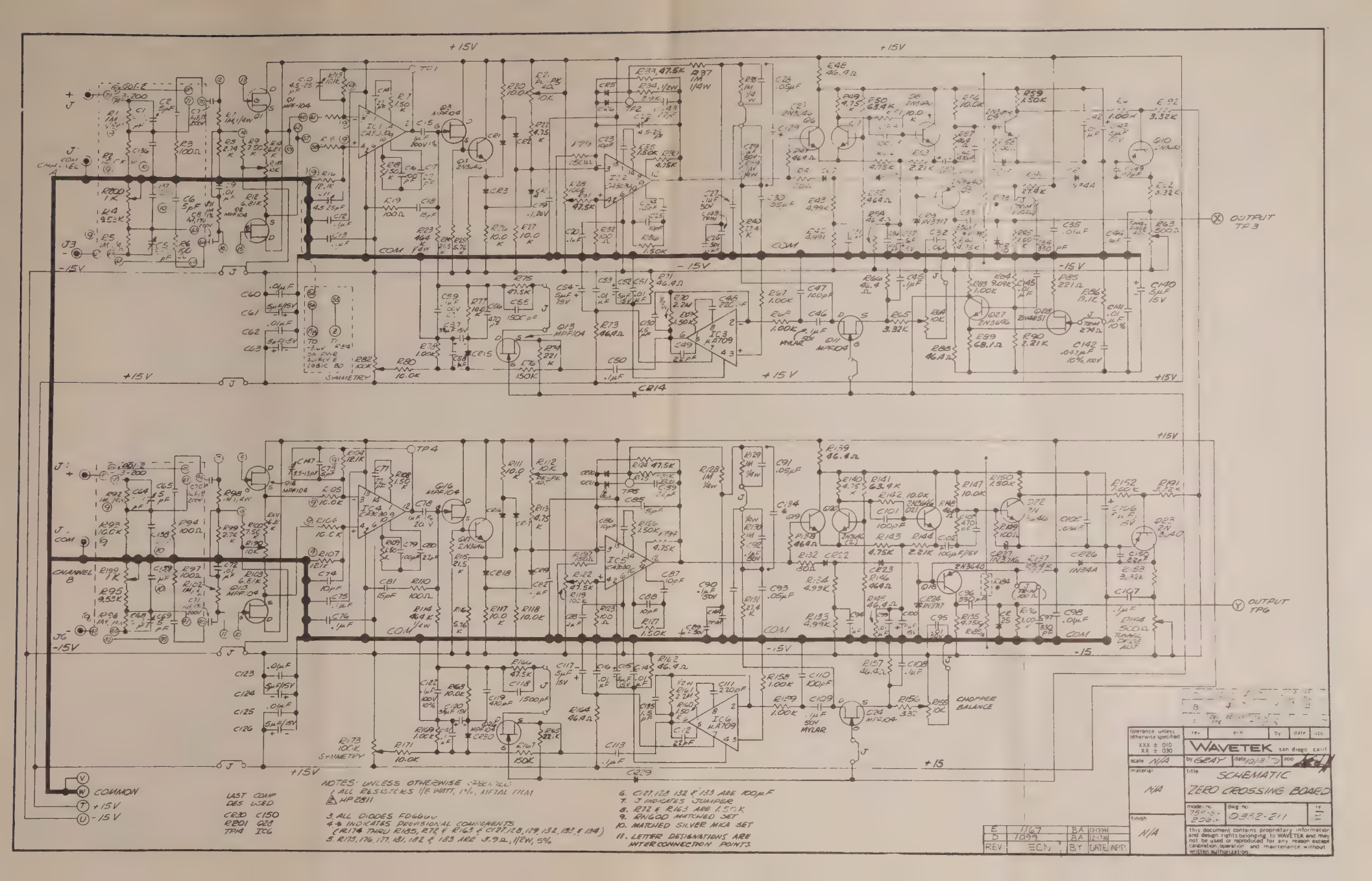
+15V
-15V
COM
COMMON
OUTPUT TP3
OUTPUT TP6
CHOPPER BALANCE
SYMMETRY
CHANNEL A
CHANNEL B
NOTES: UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTORS 1/8 WATT, 1%, METAL FILM
2. HP2811
3. ALL DIODES FD666.
4. * INDICATES PROVISIONAL COMPONENTS (R174 THRU R185, R72 & R143 & C127,128,129,132,133 & 134)
5. R175,176,177,181,182 & 183 ARE 3.9Ω, 1/2W, 5%
6. C127,128,132 & 133 ARE 100μF
7. J INDICATES JUMPER
8. R72 & R143 ARE 4.53K
9. R49,G20 MATCHED SET
10. MATCHED SILVER MICA SET
11. LETTER DESIGNATIONS ARE INTERCONNECTION POINTS
LAST COMP DES USED
C220 C150
R201 Q28
TP19 IC6
E 1167 BA 12-17-74
D 1099 BA 12-17-74
REV ECN BY DATE APP.
tolerance unless otherwise specified XXX ± .010 XX ± .030
WAVETEK san diego calif
scale N/A
by GRAY date 12/18/74 app
material N/A
finish N/A
title SCHEMATIC ZERO CROSSING BOARD
model no 75F-15-220
dwg no 0352-E11
rev
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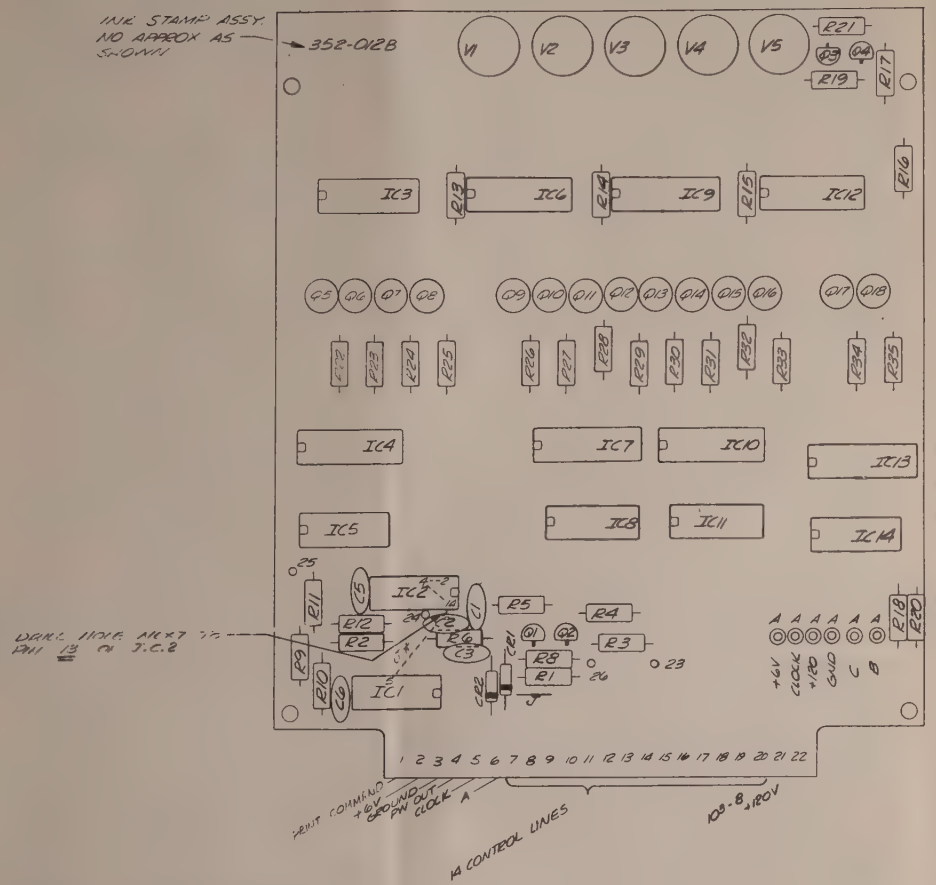

NOTES: UNLESS OTHERWISE SPECIFIED

1. CAPS MUST HAVE STRAIGHT LEADS
2. J# INDICATES JUMPER MOUNTED ON CIRCUIT SIDE

PARTS LIST

ITEM	REF DES	DESCRIPTION	MFGR	MFGR NO.	QTY
1		CAPACITORS			
2	C1, C2, C3, C6	CERAMIC DISC, 1KV, 10%, .01μF	CRL	DD102	4
3					
4	C5	10V 0.47μF	SPRAGUE	UK10-474	1
5					
6					
7					
8					
9		DIODES			
10	CR1, CR2	FD6666	FAIRCHILD	FD6666	2
11					
12					
13					
14		INTEGRATED CIRCUITS			
15	IC2	QUAD 2 INPUT NAND	MOTOROLA	SN7400	1
16	IC3, IC6, IC9, IC12	DECODER DRIVER		7441	4
17	IC4, IC7, IC10, IC13	QUAD LATCH		7475	4
18	IC5, IC8, IC11, IC14	DECADE COUNTER		7490	4
19	IC1	3 LEAD NAND BUFF		7437	1
20					
21					
22	V1-V4	NIXIE TUBES 0-9		[illegible]	4
23	V5	+, -		[illegible]	1
24					
25		RESISTORS			
26	R1, R3, R11, R12	METAL FILM 1/8W 1% 2.21K	CORNING	RN55D	4
27	R5	4.75K			1
28	R6, R20	10.0K			2
29	R13-R17	13.2K			5
30	R9, R10	47.5K			2
31	R2, R4, R7, R8	750Ω			4
32	R19, R21	1/6W, 1M		RN60D	2
33	R22-R35	1/8W 2.00K		RN55D	14
34					
35					
36					
37	Q1, Q2	TRANSISTORS 2N3646	MOTOROLA	2N3646	2
38	Q3, Q4	MPS L01		MPS L01	2
39	Q5-Q18	2N3642	FAIRCHILD	2N3642	14
40					
41					
42					
43	⊙ A	AMP PINS	AMP	61182-2	6
44					
45					
46					
47					
48		DIGITAL BOARD	WAVETEK	750-112A	1
49					
50					

rev	ecn	by	date	app
C		11.3	3A	[illegible]
B	ECN 193	AS	[illegible]	
A	E.C.N. 139			

tolerance unless otherwise specified: XXX ± .010, XX ± .030

WAVETEK san diego, calif

scale N/A | by SRA | date 3/22/70 | app [illegible]

material: N/A

title: ASSY DIGITAL BOARD

finish: N/A

model no. 75-5-300 | dwg no. 750-112 | rev C

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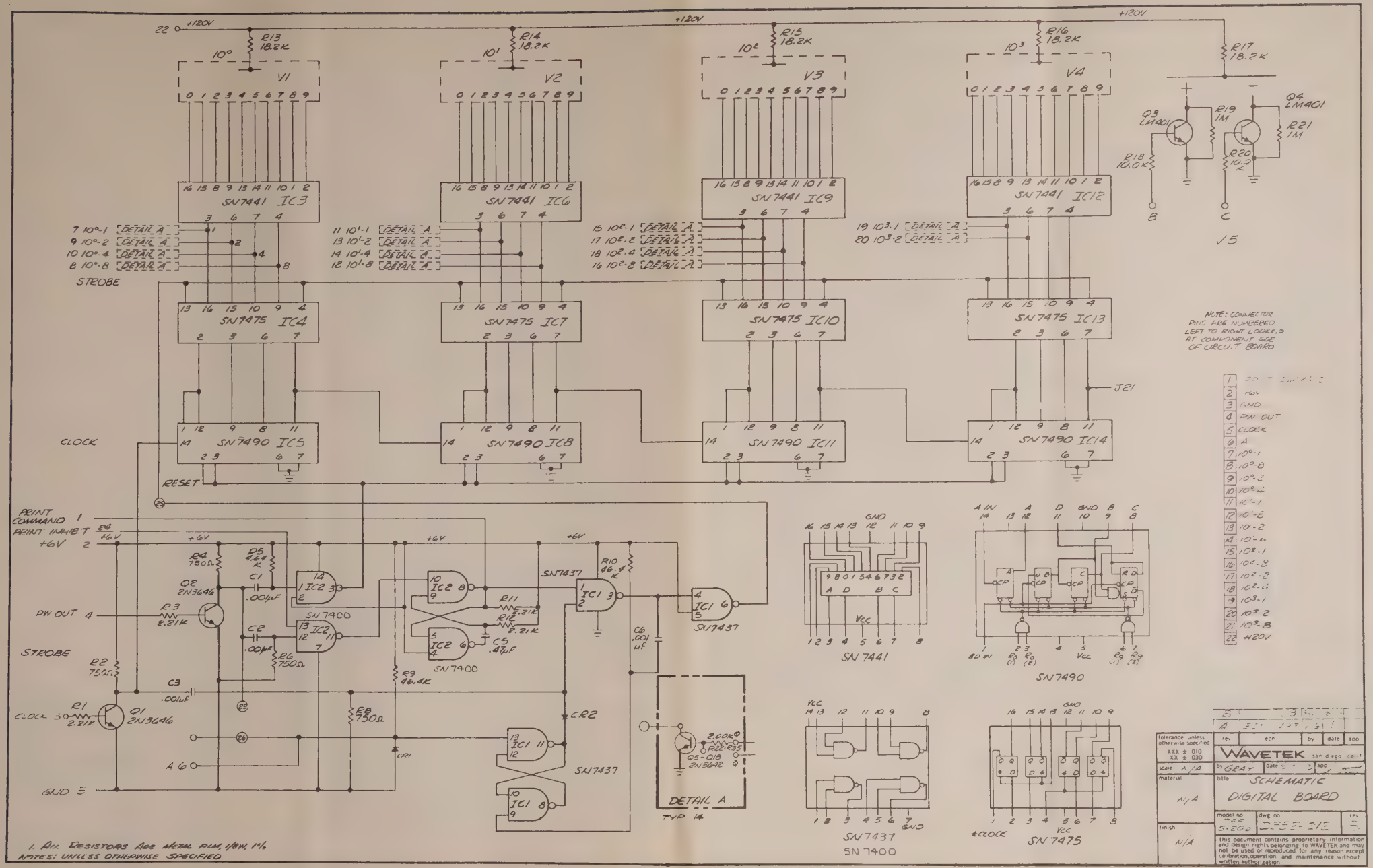
+120V
R13 18.2K
R14 18.2K
R15 18.2K
R16 18.2K
R17 18.2K
V1
V2
V3
V4
SN7441 IC3
SN7441 IC6
SN7441 IC9
SN7441 IC12
SN7475 IC4
SN7475 IC7
SN7475 IC10
SN7475 IC13
SN7490 IC5
SN7490 IC8
SN7490 IC11
SN7490 IC14
Q3 LM401
Q4 LM401
R18 10.0K
R19 1M
R20 10.2K
R21 1M
STROBE
CLOCK
RESET
PRINT COMMAND 1
PRINT INHIBIT 24
+6V
PW OUT 4
Q1 2N3646
Q2 2N3646
R1 2.21K
R2 750Ω
R3 2.21K
R4 750Ω
R5 4.64K
R6 750Ω
R7 750Ω
R8 750Ω
R9 46.4K
R10 46.4K
R11 2.21K
R12 2.21K
C1 .001μF
C2 .001μF
C3 .001μF
C5 .47μF
C6 .001μF
SN7400
SN7437
CR1
CR2
A 6
GND 5
DETAIL A
TYP 14
2.00K
R22-R25
Q5-Q18 2N3642
SN7441
SN7490
SN7437
SN7400
SN7475
*CLOCK
J21
NOTE: CONNECTOR PINS ARE NUMBERED LEFT TO RIGHT LOOKING AT COMPONENT SIDE OF CIRCUIT BOARD
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22
+6V
GND
PW OUT
CLOCK
A
10°-1
10°-8
10°-2
10°-4
10¹-1
10¹-8
10¹-2
10¹-4
10²-1
10²-8
10²-2
10²-4
10³-1
10³-2
+120V
1. ALL RESISTORS ARE METAL FILM, 1/8W, 1%
NOTES: UNLESS OTHERWISE SPECIFIED
tolerance unless otherwise specified
XXX ± 010
XX ± 030
scale N/A
material N/A
finish N/A
WAVETEK san diego calif
by GRAY
title SCHEMATIC DIGITAL BOARD
model no. 5200
dwg no. 5200-210
rev E
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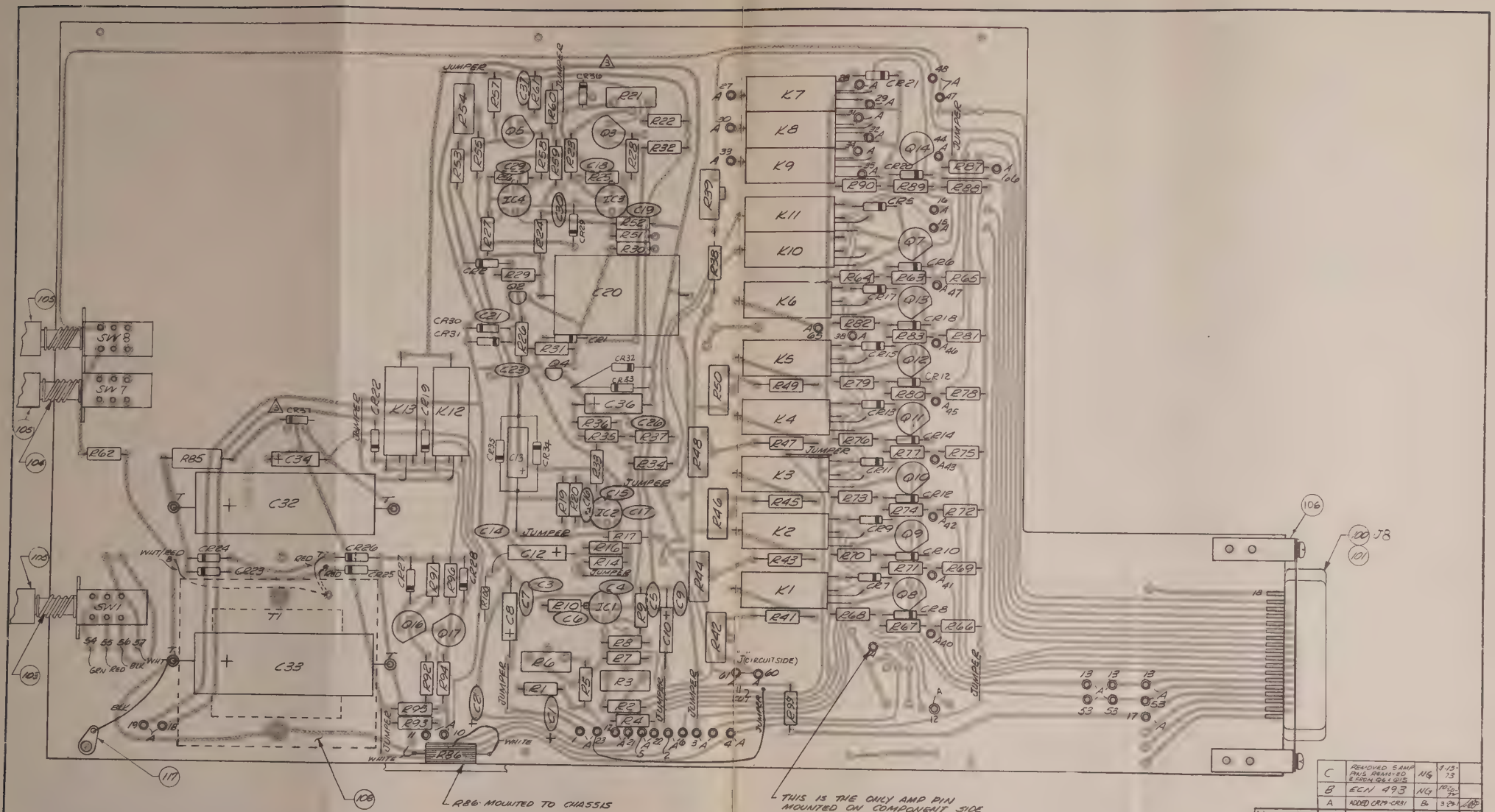

R86 MOUNTED TO CHASSIS

THIS IS THE ONLY AMP PIN MOUNTED ON COMPONENT SIDE

NOTES: UNLESS OTHERWISE SPECIFIED

1. NUMBERED AND LETTERED TERMINATIONS ARE FOR WIRING PURPOSES. SEE SCHEMATIC D352-200
2. AMP PINS ARE MOUNTED ON CIRCUIT SIDE
3. HAND BEND LEEDS ON DIODES TO FIT TRANSISTOR HOLES.

rev	ecn	by	date	app
C	REMOVED 5 AMP PINS MARKED FOR EATON CELLS	NG	9-13-73	
B	ECN 493	NG	10-22-73	
A	ADDED CR29-CR31	BA	3-29-74	

tolerance unless otherwise specified: XXX ± 010, XX ± 030

scale 2/1

material: N/A

finish: N/A

WAVETEK san diego ca if

by GRAY date 9-19-73 app

title: SHEET 1 OF 2 ASSY PHASE LOCK BD.

model no 255-5-206A

dwg no D352-014

rev D

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D 1169 BA 12-18-74

PARTS LIST

ITEM	REF DES	DESCRIPTION	MFGR	MFGR NO.	QTY
1		CAPACITORS			
2	C4, C15	CERAMIC DISC, 1000V 1% 220μF	CRL	CK221	2
3	C37	10V, 10% 1μF		UK10-104	1
4	C3, C5, C7, C9, C14, C17, C18, C19, C29, C30	50V .06μF		CK103	10
5	C6, C16, C21, C23	.005μF		CK502	4
6					
7	C12, C13, C26	TANTALUM .47μF	HARRISON ELEC	KR47W35K	3
8					
9	C20	MYLAR 200V, 1% .4μF	TRW	X663F	1
10	C8, C10, C34	ELECTROLYTIC 16V, 5μF	SPRAGUE	5000505GGN5A1	3
11	C36	10μF		TE1204	1
12	C1, C2	TANTALUM 15V, 10% 22μF		MAD226K0015F6	2
13	C32, C33	ELECTROLYTIC, 35V, 1000μF		36-750-1000-35T	2
14					
15					
16					
17					
18		DIODES			
19	CR1, CR2, CR4, CR5, CR6, CR7, CR8, CR32, 35	FD6666	FAIRCHILD	FD6666	26
20	CR22-CR26	SCE-1	SEMI-TECH	SCE-1	4
21	CR29	IN750	DICKSON	DZ7106-08A	1
22	CR30, 31		DICKSON	IN4581	2
23	CR33 to CR37	ZENER	WVTK	A130-506	2
24		INTEGRATED CIRCUIT			
25	IC1, IC2	μA709	FAIRCHILD	μA709	2
26	IC3, IC4	μA710		μA710	2
27					
28					
29					
30		POTENTIOMETER			
31	R6	500Ω	CRL	BA1603-802	1
32	R3, R21 R50, R54	1K		-803	4
33	R45, R46 R39	10K		-805	3
34	R44, R48	5K		-804	2
35					
36	R86	PWR RESISTOR, M.W. 3W, 3% 100Ω	DALE		1
37					
38		RESISTORS			
39	R61	METAL FILM, 1/8W, 1% 5612Ω	CORNING	RN55D	1
40	R59	76.7Ω			1
41	R1, R62, R87	249Ω			3
42	R60	274Ω			1
43	R34	453Ω			1
44	R51, R52	464Ω			2
45	R26	576Ω			1
46					
47					
48					
49					
50	R23, R24, R27, R28, R36, R55, R88, R99, R176	1.00K			9
51	R10, R20	1.50K			2

PARTS LIST

ITEM	REF DES	DESCRIPTION	MFGR	MFGR NO.	QTY
52		RESISTORS			
53	R65, R66, R69, R72, R75, R78, R81, R84, R93, R95, R100	METAL FILM 1/8W 1% 1.78K	CORNING	RN55D	11
54	R63, R67, R71, R74, R77, R80, R83, R89, R92, R94	2.00K			10
55	R9	3.32K			1
56	R22, R53	4.75K			2
57	R35, R37	5.76K			2
58	R5	9.53K			1
59	R7, R8, R32, R57	10.0K			4
60	R17, R16	15.0K			2
61	R2, R4, R91, R96	21.5K			4
62	R64, R68, R70, R73, R76, R79, R82, R90	24.9K			8
63	R25, R56	47.5K			2
64	R38	95.3K			1
65	R29, R31	221K			2
66	R19	237K			1
67					
68					
69	R49	1/4W, 19.6K		RN60D	1
70	R43, R47	1/8W 38.3K			2
71	R41, R45	1/4W 115K			2
72					
73					
74	R30	CARBON, 1/2W, 10% 560K	STACKPOLE	RC20GF564K	1
75	R33	680K		684K	1
76					
77					
78	R85	1W, 5% 560Ω		RC40GF561J	1
79					
80					
81					
82					
83					
84		TRANSISTORS			
85	Q1-Q14	2N3638A	FAIRCHILD	2N3638A	8
86	Q3, Q5, Q16, Q17	2N3638			4
87	Q2, Q4	(FET) 2N5458	MOTOROLA	2N5458	2
88					
89					
90					
91					
92		RELAYS			
93	K1-K6, K10-K13	FORM A	JENCO	RR30-1024	10
94	K7-K9	C		-1023	3
95					
96					
97		CONNECTORS			
98		36 PIN PLUG	AMPHENOL	57-30360	1
99		36 PIN SOCKET		57-40360	1
100					
101					

PARTS LIST

ITEM	REF DES	DESCRIPTION	MFGR	MFGR NO	QTY
102		SWITCHES			
103	SW1	PUSH PUSH AC	WAVETEK	B740-400	1
104	SW2 SW3	DUAL DPDT	WAVETEK	B750-400	2
105		PUSHBUTTON		J52305 BLK	3
106		CONN. MTG BLOCK	WAVETEK	A157-315	2
107					
108	T1	TRANSFORMER	WAVETEK	C130-500	1
109		STANDOFF 9/16	WAVETEK	A003-013-1	2
110					
111		BRACKET	WAVETEK	A755 324	2
112		P.C. BOARD	WAVETEK	755-114C	1
113					
114	◎T	TERMINALS	USECO	20108	4
115					
116	◎ A	AMP PINS	AMP	61182-2	55
117		SOLDER LUG #4			
118					
119					
120					

rev	ecn	by	date	ppc
D	1169	BA	12-18-74	
C		NG	7-15-74	
B	ECN 493	NG	7-2-74	
A	Assoc SCH-31	BA	3-27-74	

tolerance unless otherwise specified: XXX ± 010, XX ± 030

WAVETEK san diego, calif.

scale N/A | by GRAY | date 9/18/73 | ASS'Y [illegible]

material: N/A

title: SHEET 2 OF 2 ASSY PHASE LOCK BD.

finish: N/A

model no. 755-5-200A | dwg no. D352-014 | rev D

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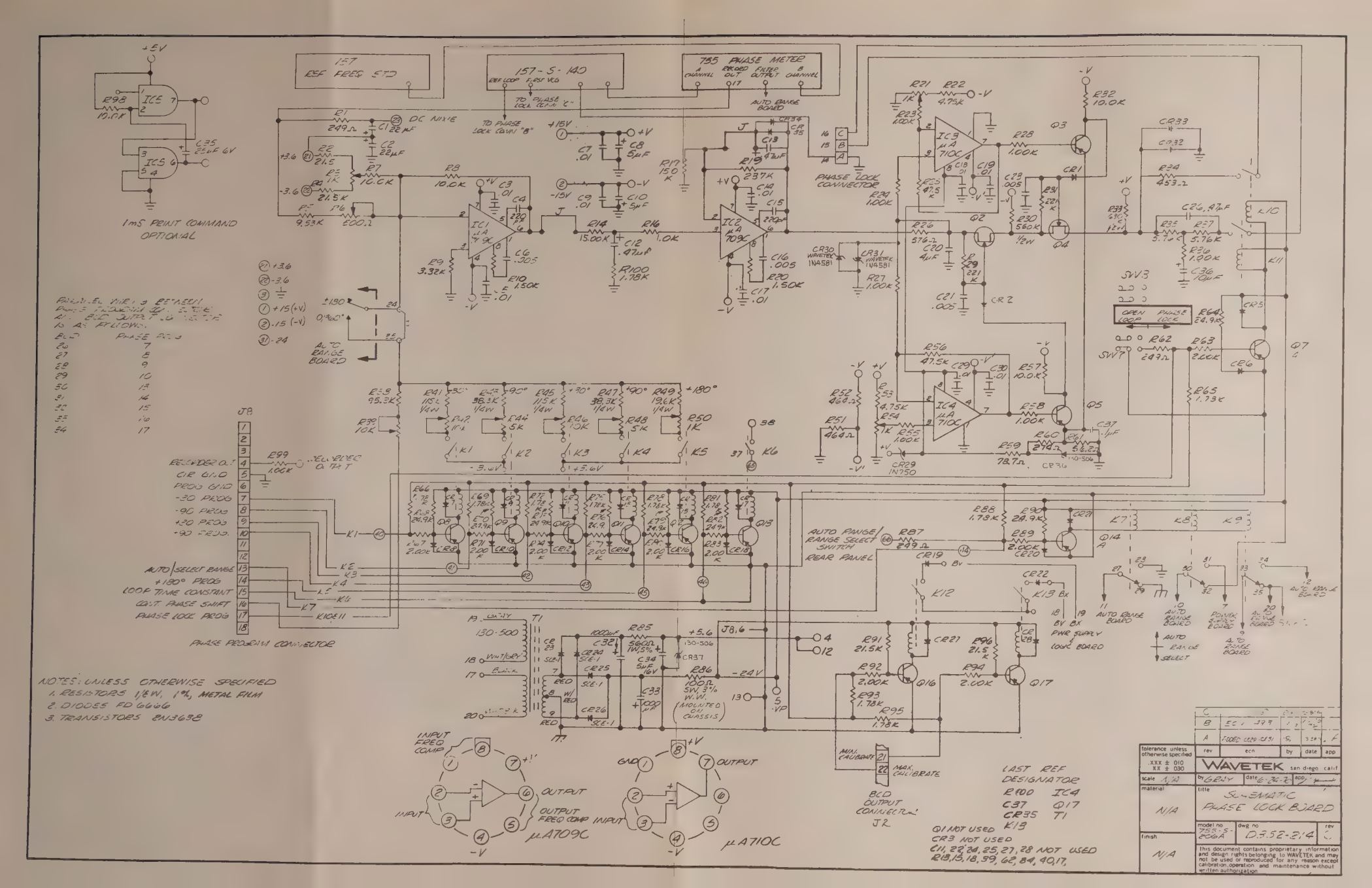
157 REF FREQ STD
157-S-140
755 PHASE METER
TO PHASE LOCK CONN "B"
TO PHASE LOCK CONN "C"
AUTO RANGE BOARD
PHASE LOCK CONNECTOR
DC NIXIE
1mS PRINT COMMAND OPTIONAL
AUTO RANGE BOARD
OPEN LOOP
PHASE LOCK
SW3
SW7
AUTO RANGE/ RANGE SELECT SWITCH REAR PANEL
PHASE PROGRAM CONNECTOR
BCD OUTPUT CONNECTOR J2
PWR SUPPLY LOGIC BOARD
AUTO RANGE SELECT
POWER SUPPLY BOARD
μA709C
μA710C
INPUT FREQ COMP
OUTPUT
OUTPUT FREQ COMP
INPUT
GND
MAX. CALIBRATE
MIN. CALIBRATE
AUTO/SELECT RANGE
+180° PROG
LOOP TIME CONSTANT
QUIET PHASE SHIFT
PHASE LOCK PROG
RECORDER O/P
CIR O/P
PROG O/P
-30 PROG
-90 PROG
+30 PROG
+90 PROG
SELECTED O/P
LAST REF DESIGNATOR
R100 IC4
C37 Q17
CR35 T1
K13
Q1 NOT USED
CR3 NOT USED
C11, 22, 24, 25, 27, 28 NOT USED
R13, 15, 18, 39, 62, 84, 90, 17,
NOTES: UNLESS OTHERWISE SPECIFIED
1. RESISTORS 1/8W, 1%, METAL FILM
2. DIODES FD6666
3. TRANSISTORS 2N3638
WAVETEK san diego calif
SCHEMATIC
PHASE LOCK BOARD
D.S.52-2.14
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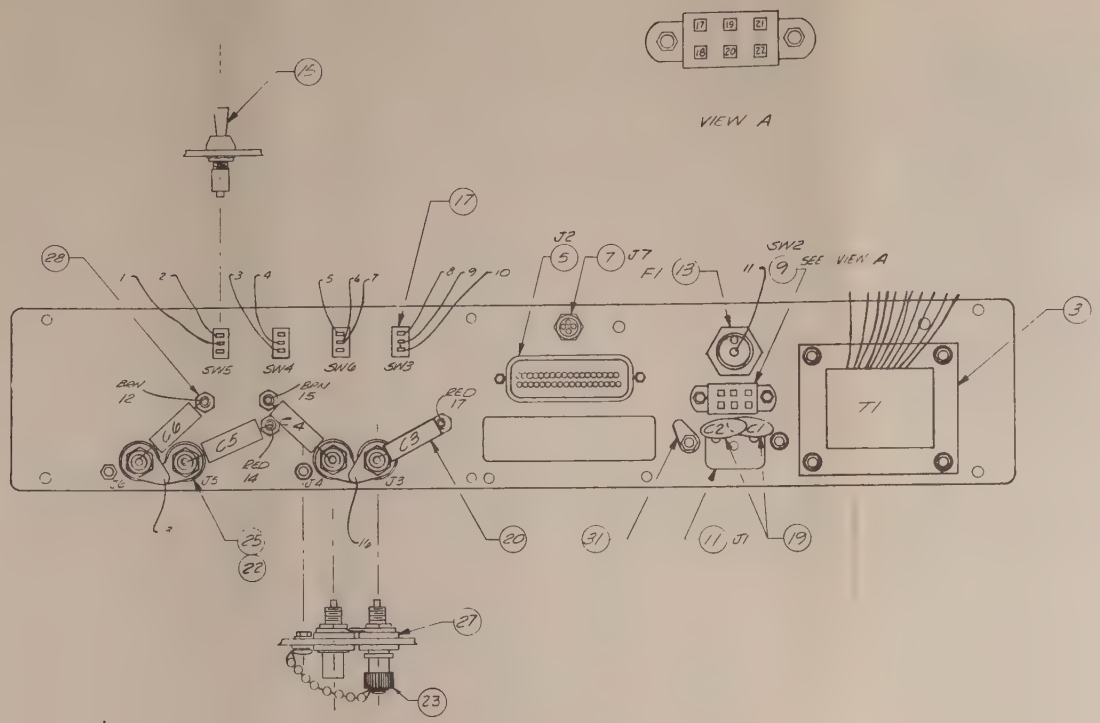

PARTS LIST

ITEM	REF DES	DESCRIPTION	MFGR	MFGR NO	QTY
1		REAR PANEL	WAVETEK	C552-600	1
2					
3	T1	TRANSFORMER	WAVETEK	0750-565	1
4					
5	J2	CONNECTOR, SOCKET	AMPHENOL	57-40500	1
6		PLUG	"	57-30360	1
7	J7	CONNECTOR, PHASE LOCK	AMPHENOL	29-204-001	1
8			"	29-205	1
9	SW2	LINE SWITCH	OAK	A14SA-2	1
10					
11	J	POWER ENTRY			1
12					
13	F1	FUSE 1/8A SLO	TYE-PLUSE	3-2-3-1	1
14					
15	SW4-SW6	SWITCH	C&K	7101-M-203	3
16					
17	SW3	SWITCH	C&K	7105-T-203	1
18					
19	J2	CONNECTOR D.S. MALE			2
20	C3-C6	MYLAR 200V .1uF			4
21					
22	J3-J6	BNC CONNECTOR		31-73	4
23		SHORTING CAP			3
24					
25		BUSHING			4
26					
27		BUSHING		31-3	9
28		TERMINAL		28-2	4
29		FUSE 1/8A SLO			2
30		230 V 4 WIRE			1
31		SOCKET		31-4	1

REV	ECN	BY	DATE	APP.
C	165	BF	12-7	
A	SURFACE BRACKET HOLES ADDED	WU	3-2-	

tolerance unless otherwise specified: XXX ± .010, XX ± .030
scale: FULL
material: N/A
finish: N/A

WAVETEK san diego, calif.

by: BRET date: 7/1/70 app:

title: (REAR PANEL)

model no: 756-5-804 dwg no: D0756-6600 rev: -

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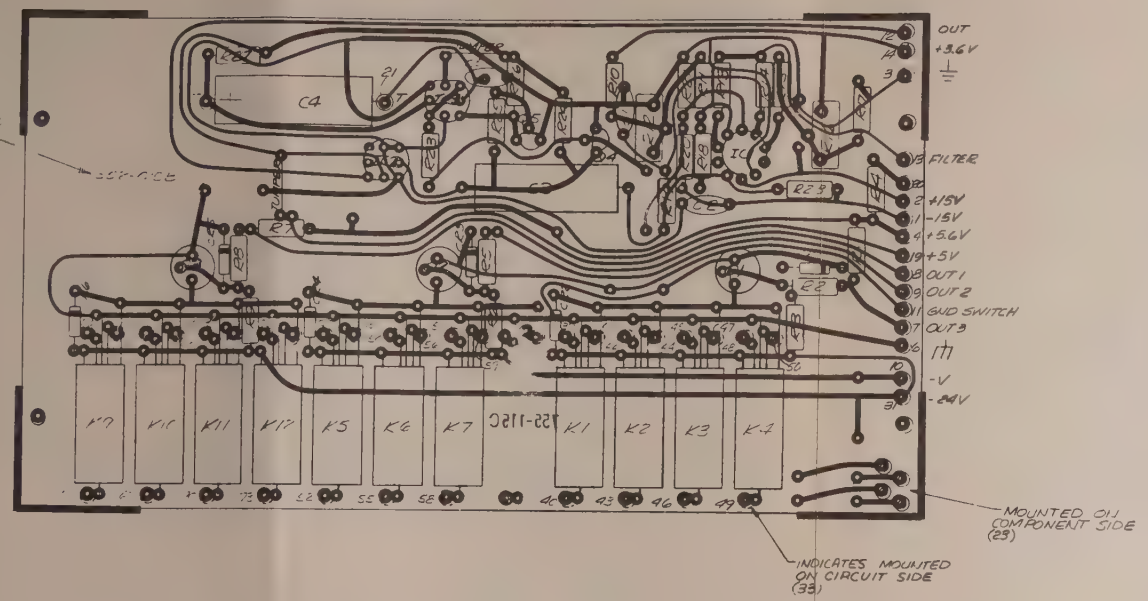

PARTS LIST

ITEM	REF DES	DESCRIPTION	MFGR	MFGR NO	QTY
1		CAPACITOR			
2	C1, C2	CERAMIC DISC, 20V .1μF	CRL	UK20-104	2
3	C3	MYLAR 200V 1μF	ELECTRO CUBE	210BIC-105F	1
4	C4	ELECTROLYTIC 12V, 200mF	SPRAGUE	TE 1137	1
5	C5	CERAMIC DISC, 1K 470pF	CRL	DC471	1
6					
7					
8					
9	CR1-CR6	DIODE FD6666	FAIRCHILD	FD6666	6
10					
11					
12		INTEGRATED CIRCUITS			
13	IC1	DUAL COMPARATOR	FAIRCHILD	μA711	1
14	IC2	DUAL INPUT GATE		μL923	1
15	IC3	JK FLIP FLOP		μL914	1
16					
17					
18					
19	K1-K11 K9-K12	RELAY FORM C	JENCO	R30-1023	11
20					
21					
22	Q1 Q2, Q3	TRANSISTOR 2N3638A	FAIRCHILD	2N3638	3
23	Q4 Q5	2N3646		2N3640	2
24					
25					
26		RESISTOR			
27	R20, R21	METAL FILM 1/8W, 1%, 464Ω	CORNING	CEA	2
28	R15, R23	511Ω			2
29	R1, R3, R4, R13, R25	1.00K			5
30	R7, R24, R27, R28	1.78K			4
31	R2, R5, R8, R26	2.00K			4
32	R10, R17	4.99K			2
33	R22	0.0Ω			1
34	R3, R6, R9	21.5K			3
35	R18, R19	47.5K			2
36					
37					
38					
39					
40	R11, R16	POTENTIOMETER 1K	CRL	BA1603-B03	2
41					
42	T	TERMINALS	USECO	[illegible]	[illegible]
43	(10) (0)	AMP PINS	AMP	41182-2	55
44		TRANSIPADS (Q1, Q2, Q3)	MILTON ROSS	TO 23N	3
45					
46		CIRCUIT BOARD	WAVETEK	755 151	1
47					
48					
49					
50					

tolerance unless otherwise specified XXX ± .010 XX ± .030

scale N.A.

material I. A

finish N/A

rev | e.n | D. | date | appd

WAVETEK

drawn | date 3-1 | tool

title A.E.I.B.L. AUTO RANGE BD

model no 75,9-5-806A

dwg no 0352-6405 rev E

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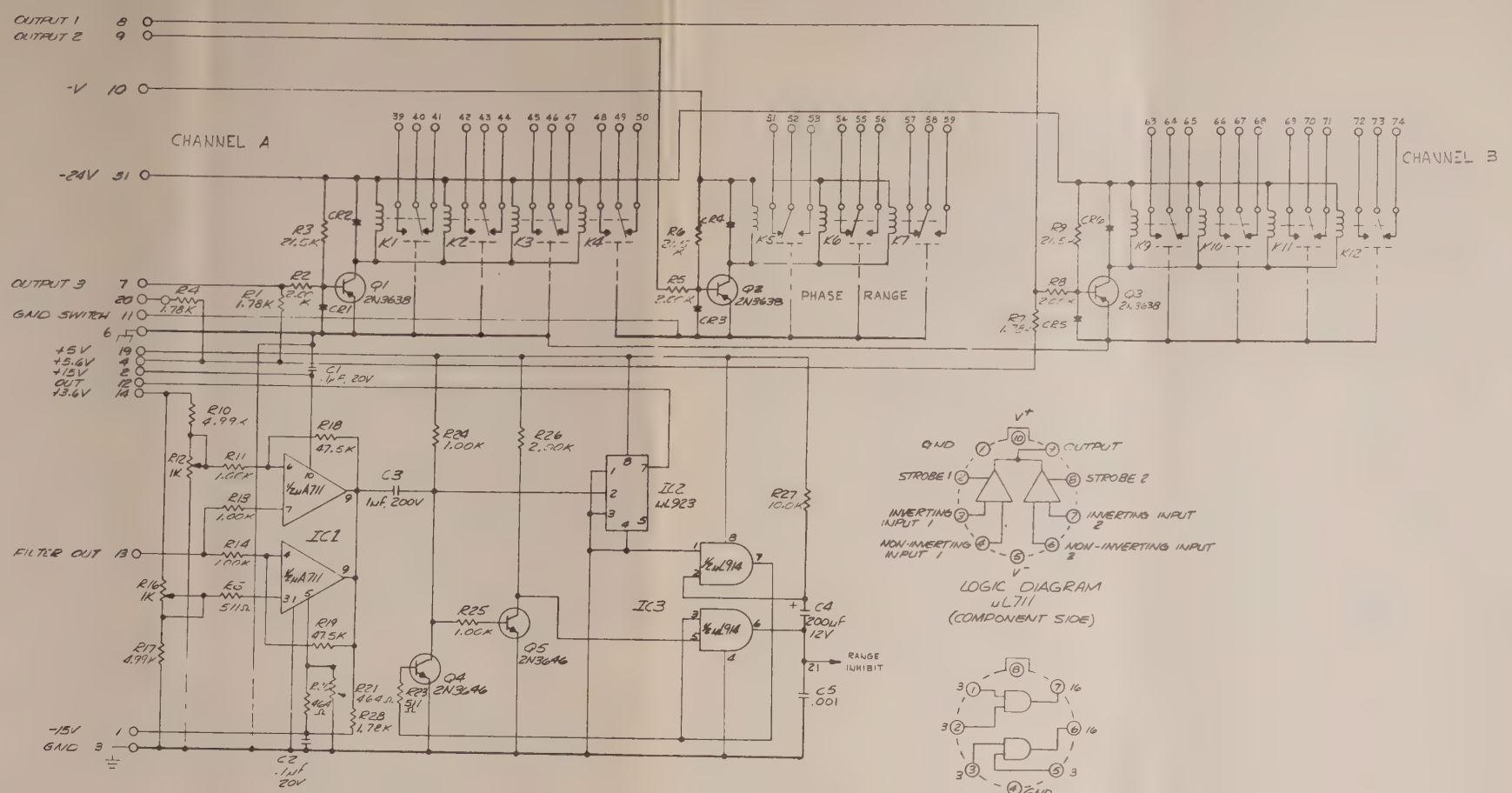
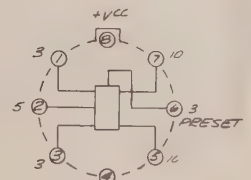


LOGIC DIAGRAM
μL711
(COMPONENT SIDE)

LOGIC DIAGRAM
μL914
(COMPONENT SIDE)



LOGIC DIAGRAM
μL923
(COMPONENT SIDE)

NOTES UNLESS OTHERWISE SPECIFIED

1. RESISTORS ARE METAL FILM, 1/8W, 1%
2. DIODES ARE FD6666
3. RELAYS ARE JENCO R30-1023 OR EQUIV

	rev	ecn	by	date	app
tolerance unless otherwise specified XXX ± .010 XX ± .030	WAVETEK san diego, calif				
scale N/A	by BOCHKHIS	date 4-18-70	app		
material N/A	title SCHEMATIC AUTO RANGE BD				
finish N/A	model no 755-5 2034	dwg no D755-E1-5		rev B	

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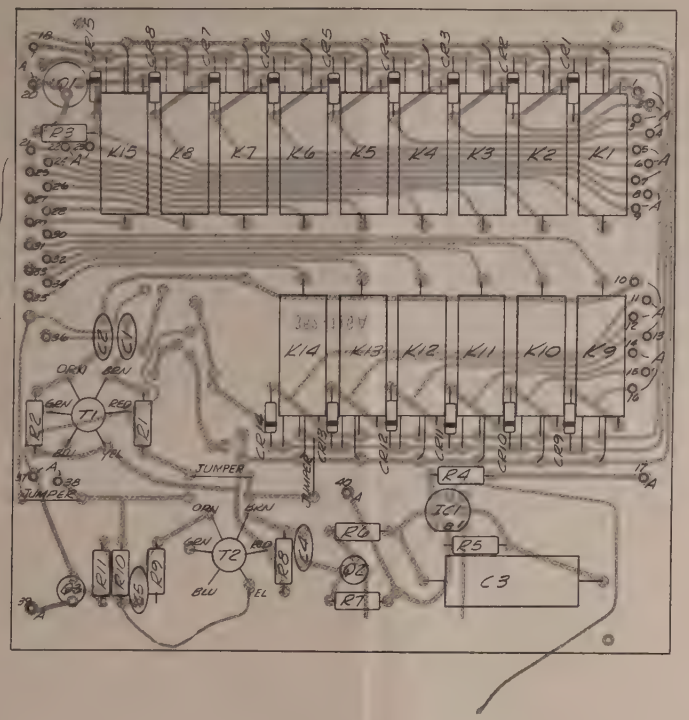

NOTE: AMP PINS INSTALLED ON COMPONENT SIDE

PARTS LIST

ITEM	REF DES	DESCRIPTION	MFGR	MFGR NO	QTY
1		CAPACITORS			
2	C1, C2	CERAMIC DISC, 1000V, 10%, .001μF	CRL	DD102	2
3	C4, C5	50V, 10%, .01μF	〃	CK-103	2
4	C3	MYLAR, 200V, 10% 2μF	AMERICAN RAD.	2MEW205K	1
5					
6					
7					
8	CR1-CR15	DIODES FD6666	FAIRCHILD	FD6666	15
9					
10					
11		RESISTORS			
12	R4	METAL FILM 1/8W, 1% 100Ω	CORNING	RN55D	1
13	R6, R7, R10, R11	1.00K	〃	〃	4
14	R3	2.00K	〃	〃	1
15	R1, R2, R5, R8, R9	10.0K	〃	〃	5
16					
17					
18					
19	K1-K15	RELAYS FORM A	JENCO	RR-30-1024	15
20					
21					
22		INTEGRATED CIRCUITS			
23	IC1	μL914	FAIRCHILD	μA914	1
24					
25	T1, T2	TRANSFORMER, PULSE	UTC	PIP-5	2
26					
27					
28					
29	Q1	TRANSISTOR, NPN	FAIRCHILD	2N3642	1
30	Q2, Q3	〃 〃	〃	2N3646	2
31					
32					
33		P.C. BOARD	WAVETEK	352-116A	1
34					
35	A	AMP PINS	AMP	61182-2	39

	A	ECN # 493	JH	4/5/71
tolerance unless otherwise specified	rev	ecn	by	date app
XXX ± .010 XX ± .030	WAVETEK san diego, calif			
scale 8/1	by GRAY	date 9-22-70	app.	
material N/A	title ASSY, ISOLATION BOARD			
finish N/A	mode no 755-5-206	dwg no D352-016	rev A	

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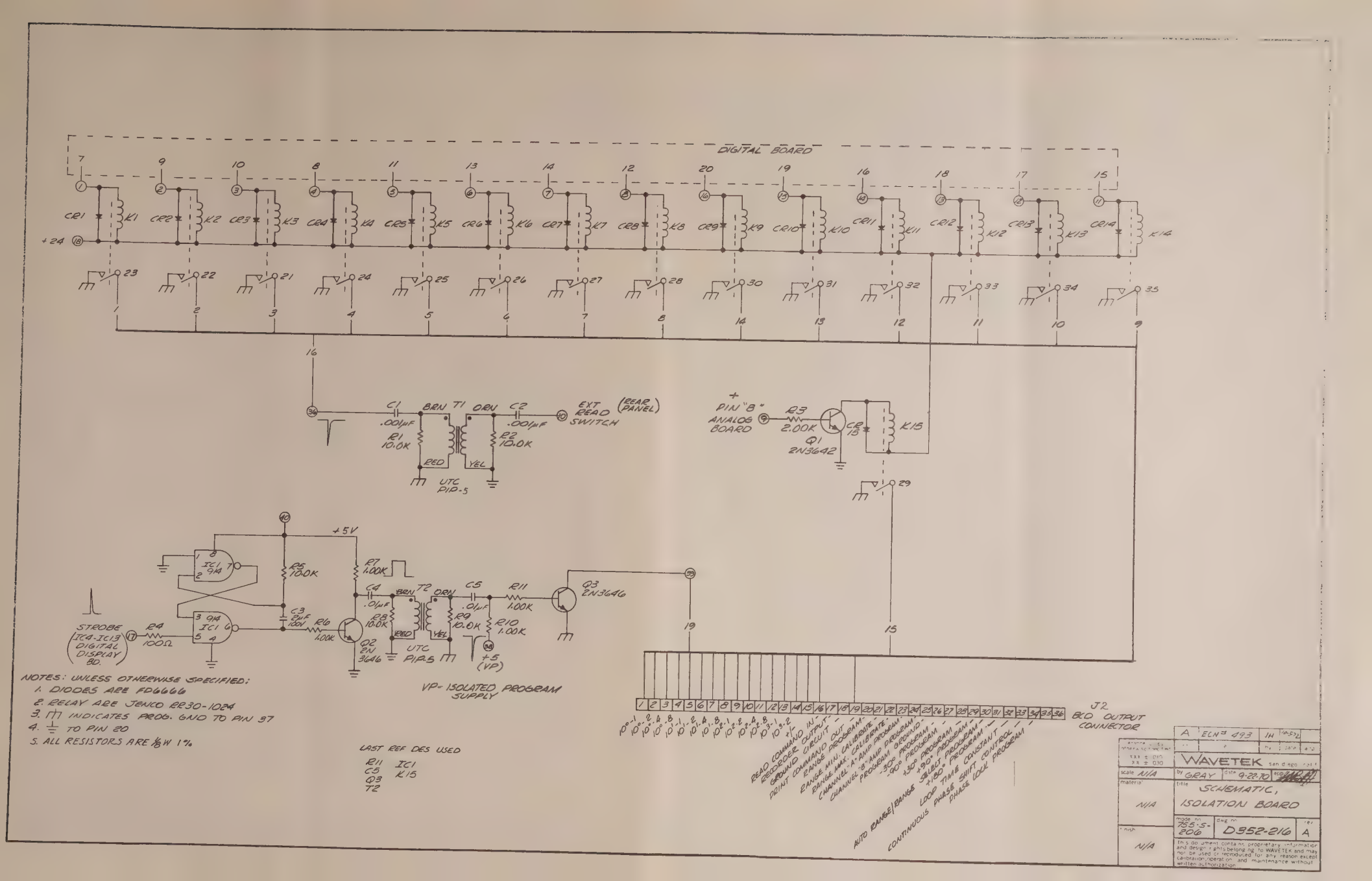

NOTES: UNLESS OTHERWISE SPECIFIED:
1. DIODES ARE FD6666
2. RELAY ARE JENCO BR30-1024
3. ⏚ INDICATES PROG. GND TO PIN 37
4. ⏚ TO PIN 20
5. ALL RESISTORS ARE ⅛W 1%

LAST REF DES USED

R11	IC1
C5	K15
Q3	
T2	

A	ECN# 493	IH	
XXX ± .010 XX ± .030	WAVETEK san diego		
scale N/A	by GRAY	date 9-28-70	approved
material N/A	title SCHEMATIC, ISOLATION BOARD		
finish N/A	model no. 755-S-206	dwg no. D352-216	rev A

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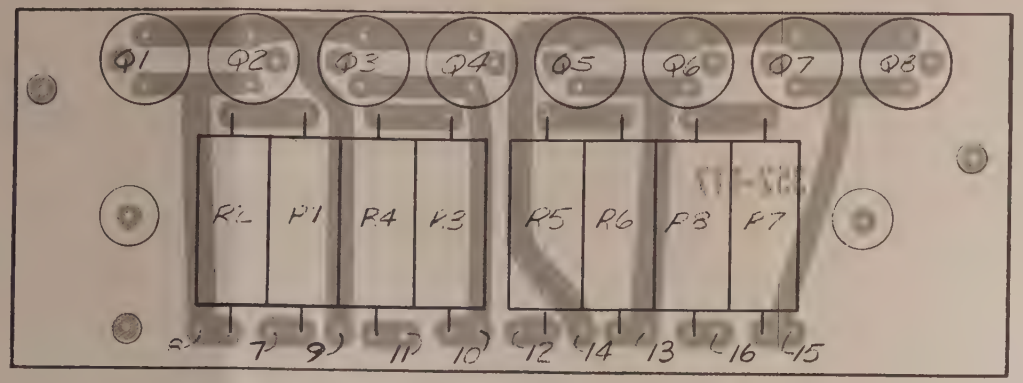

PARTS LIST

ITEM	REF DES	DESCRIPTION	MFGR	MFGR NO	QTY
1	R1-R8	RESISTOR 2W, 10% 15K	STACKPOLE	RC42GF153K	8
2					
3					
4	Q1-Q8	TRANSISTOR 2N3638	FAIRCHILD	2N3638	8
5					
6					
7		CIRCUIT BOARD	WAVETEK	352-117	1
8					
9					
10					

TOLERANCE UNLESS OTHERWISE SPEC
XXX ± .010
XX ± .030
ANGLES ± 0°30'

SCALE N/A

MATERIAL N/A

FINISH N/A

REV	ECN	BY	DATE	APP

WAVETEK SAN DIEGO CALIF

BY [illegible] DATE 3-22-71 APP

TITLE ASS'Y INPUT PROTECTION

MODEL NO 755-5-206 DWG NO 9352-017 REV

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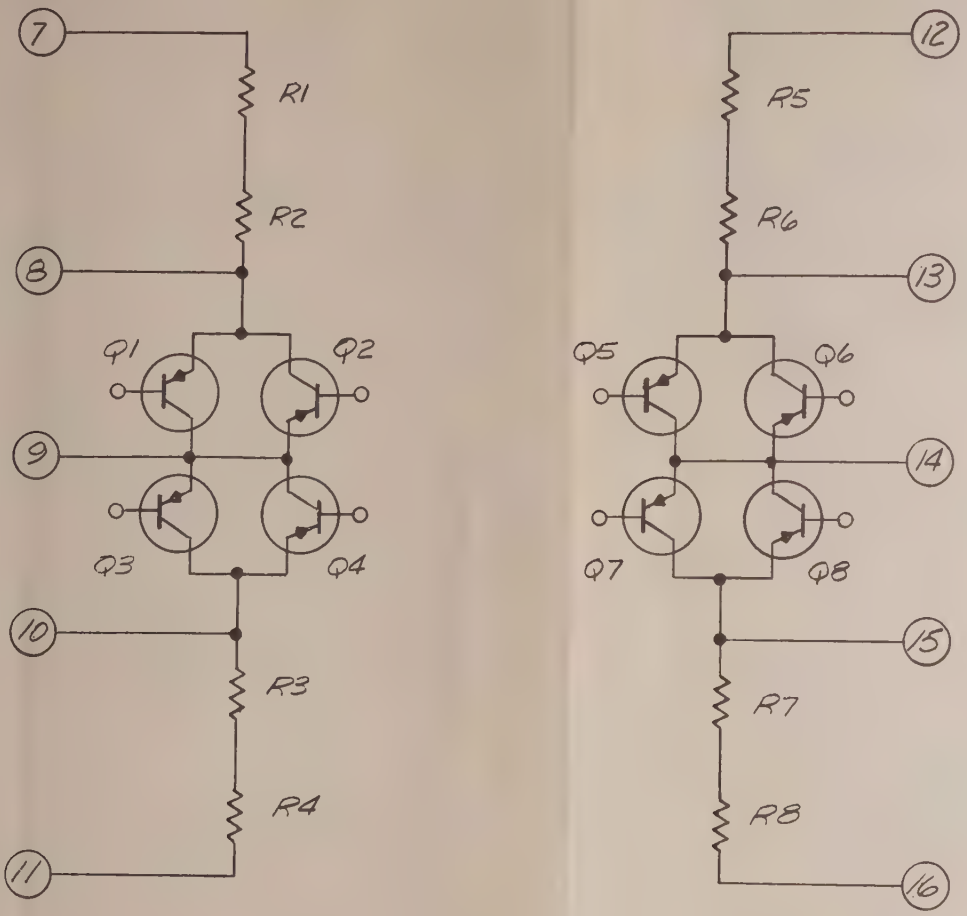

NOTES
1 RESISTORS ARE 15K 2W CARBON
2 TRANSISTORS ARE 2N3638

TOLERANCE UNLESS OTHERWISE SPEC: XXX .010, XX .030, ANGLES 0 30	REV	ECN	BY	DATE	APP
	WAVETEK SAN DIEGO, CALIF			
SCALE N/A	BY BOHKHN	DATE 9-26-71	APP	
MATERIAL N/A	TITLE SCHEMATIC INPUT PROTECTION			
FINISH N/A	MODEL NO 955-5 -206	DWG NO B352-217	REV	

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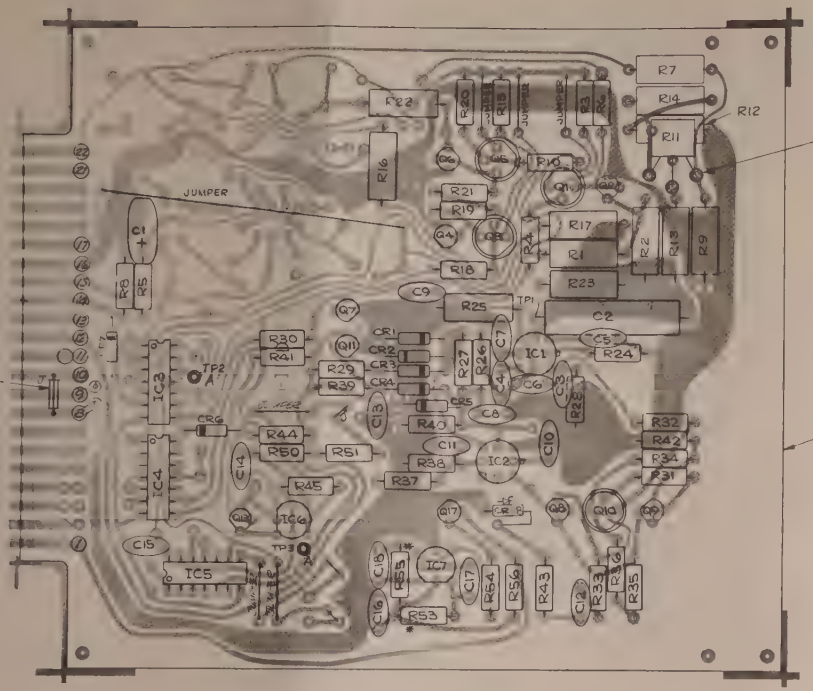

NOTES. UNLESS OTHERWISE SPECIFIED:-

1. ALL JUMPERS ARE SLEEVED.
2.
3. FOR INTERCONNECTIONS REFER SCHEMATIC D750-200
4. A INDICATES AMP PIN MOUNTED FROM NEAR SIDE.
5. NO SUBSTITUTION SHALL BE ALLOWED FOR PART NOTED.
6. * R53 & R55, MF ON STANDARD 755 ONLY
7. LETTER DESIGNATIONS ARE INTERCONNECTION POINTS.
8. ADD SLEEVE JUMPER FOR 755 & 352 ONLY

S-206 ADD JUMPER BETWEEN PINS 8 & 10.
S-271 ADD JUMPER BETWEEN PINS 9 & 10.

PARTS LIST

ITEM	REF DES	DESCRIPTION	MFG BY	MFG No.	QTY
1					
2	C4	CAPACITOR, DISC, 22 pf 1KV	CRL	DD220	1
3	C14	47 pf 1KV		DD470	1
4	C12	470 pf 1KV		DD471	1
5	C17	.0015 μfd 1KV		DD152	1
6	C18	.0022 μfd 1KV		DD222	1
7	C5, C6, C8,	.005 μfd 50V		CK502	3
8	C3, C7, C9, C10 C11, C13, C15, C16	.01 μfd 50V		CK103	8
9	C2	MYLAR 1 μfd 1% 200V	ELECTROCUBE	210-B1C-105F	1
10	C1	TANTALUM 27 μfd 35V	SPRAGUE	196D276X0035FB	1
11					
12					
13					
14					
15					
16	IC3, IC4	MC863P INTEGRATED CIRCUIT	MOTOROLA	MC863P	2
17	IC5	MC856P		MC856P	1
18	IC6, IC7	CμL914	FAIRCHILD	CμL914	2
19	IC1	μA709 (-44)		μA709	1
20	IC2	μA710		μA710	1
21					
22					
23					
24					
25					
26	CR1 THRU CR7	FD6666 DIODE	FAIRCHILD	FD6666	7
27					
28					
29					
30	Q1, Q3, Q5 Q10	2N3638 TRANSISTOR	FAIRCHILD	2N3638	4
31	Q7, Q8, Q9, Q11 Q13, Q17	2N3646		2N3646	6
32					
33	Q2, Q4, Q6	2N4250 ⚠5	FAIRCHILD	2N4250	3
34	CR8	ZENER DIODE	DICKSON	DZ7106-08A	1
35					
36					
37					
38					
39		CIRCUIT BOARD	WAVETEK	270-1111	1
40		AMP PIN	AMP	61182-2	2
41		TERMINAL	USECO	2005B-1	3
42		TRANSIPAD	MILTON ROY	10123N	3
43					

PARTS LIST

ITEM	REF DES	DESCRIPTION	MFG BY	MFG NO.	QTY
44	R5, R6	21.5Ω 1/8 WATT M.F. 1%	CORNING	RN55C	2
45	R32	82.5Ω			1
46	R28	100Ω			1
47	R33	221Ω			1
48	R37, R38	676Ω			2
49	R3, R5, R20, R36 R42, R43, R45, R54, R56	1.00K			9
50	R4, R10, R15, R26 R27, R30, R31, R40 R44, R50, R51,	2.21K			11
51	R40	4.75K			1
52	R6, R19, R21	8.25K			3
53	R29, R35, R39	10.0K			3
54	R34	63.4K			1
55					
56	R24	1.50K			1
57					
58					
59					
60	R9, R12	49.9Ω WIREWOUND (-43) 1%	MICRO OHM		2
61	R25	10K (-43)			1
62	R2, R7, R13, R14 R16, R17, R22, R23	30.1K (-43)			8
63	R1	137K (-43)			1
64					
65					
66					
67					
68	R53, R55	21.5K METAL FILM 1/8 WATT 1%	CORNING	RN55D	2
69	R53 - 75	2.1K (-43)			
70					
71					
72	R11	1K POTENTIOMETER (-43)	LB	SV1C2	1
73					
74					
75					

rev	ecn	by	date	app
H	1164	BA	12/17/74	
G	ECN 581	[illegible]	2-26-73	
F	ECN 512	[illegible]	12-4-72	S
E	ECN 493	MG	9/11/72	
D	ECN 338	S	9/11/72	S
C	ECN 317	MG	7/28/72	
B	ECN 306	MG	7/12/72	
A	ECN-294	R	12/7/71	

tolerance unless otherwise specified
XXX ± .010
XX ± .030

scale 2X

material

finish N/A

WAVETEK san diego, calif

by L. ADAMSON date 8/1/69 app

title
ASSEMBLY, ANALOG BOARD

model no 210, 352, 706, 755

dwg no D270-011

rev H

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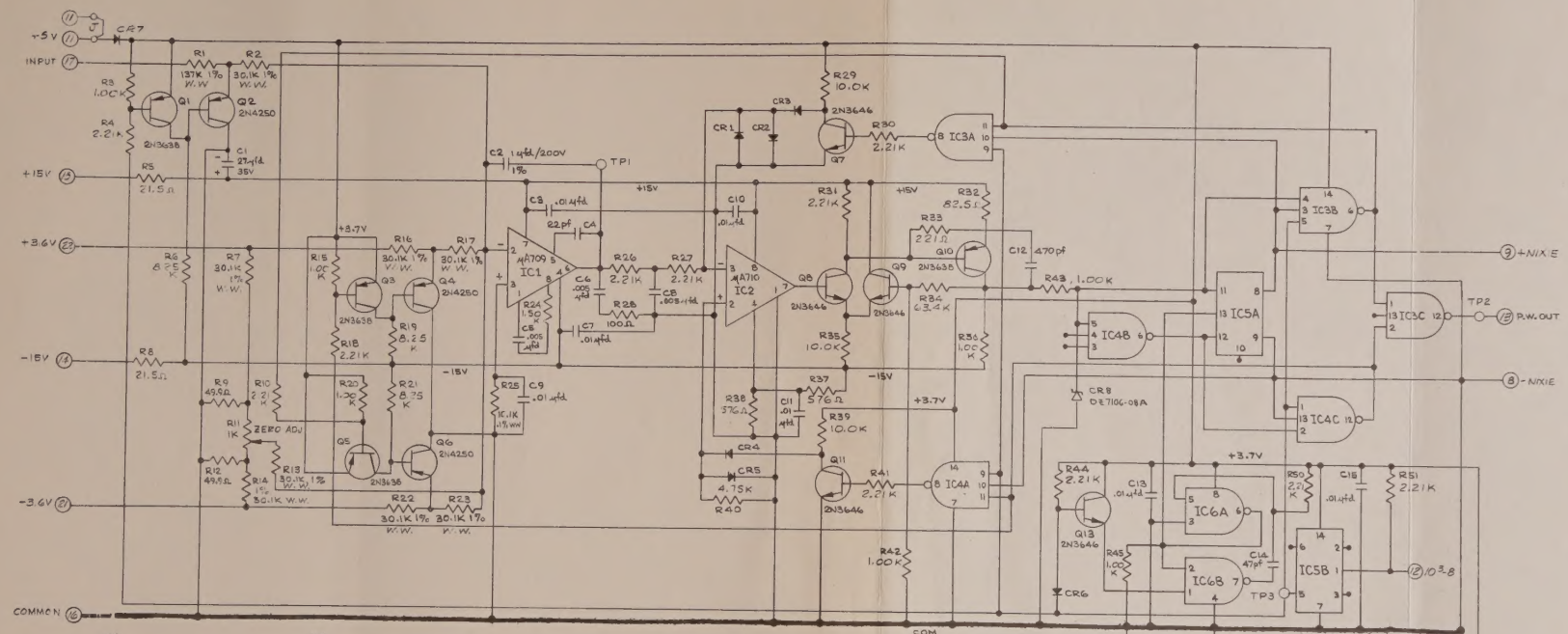

NOTES:- UNLESS OTHERWISE SPECIFIED-

1. ALL DIODES FD666
2. ALL RESISTORS 1/8 WATT, 1%, METAL FILM
3.
4.
5.
6. IC3 & IC4 ARE MC863P
7. IC5 IS MC856P
8. IC6 & IC7 ARE C4L914
9. FOR INTERCONNECTION SEE D750-200

10 * R53 & R55, 12.1K MF ON STANDARD 755 ONLY

LAST COMP DES USED
R54 TP6
C18 Q17
CR7 IC7

rev	ecn	by	date	app.
D	ECN 581	Shel	2 Sept	
C	ECN 417	NG	10 Dec.	
B	ECN 317	NG	2 Sept	
A	ECN 306	NG	7 Feb	

tolerance unless otherwise specified .XXX ± .010 .XX ± .030

scale N/A

material N/A

finish N/A

WAVETEK san diego, calif

by MAST date 28 NOV 69 app.

title SCHEMATIC, ANALOG BOARD

model no. 270, 355, 755 dwg no. D270-211 rev D

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